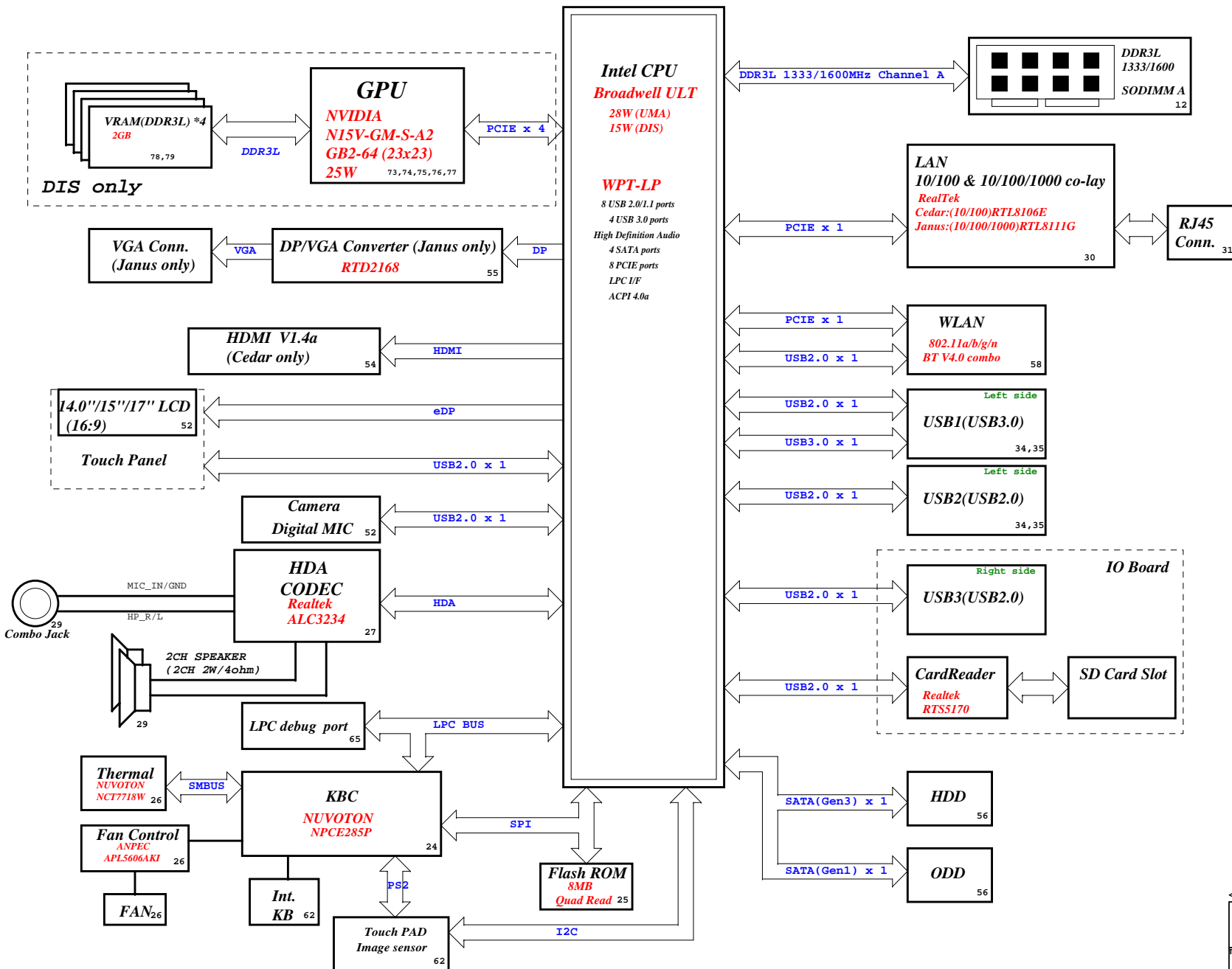


Project code:4PD00I010001
PCB P/N: 13302-1
Revision: A00

Cedar/Janus Block Diagram



(Blanking)

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Title			(Reserved)		
Size	Document Number				Rev
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Date: Friday, February 07, 2014			Sheet	3	of 104

SSID = CPU

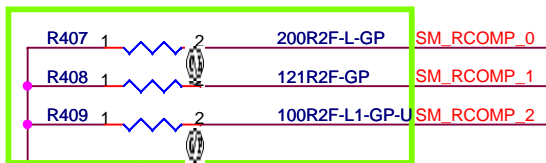
Layout Note:

Impedance control: 50 ohm

[24,42,44,46] H_PROCHOT# <<>>

[36] H_THERMTRIP_EN <<<

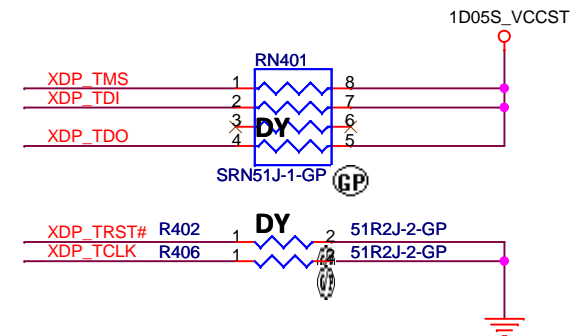
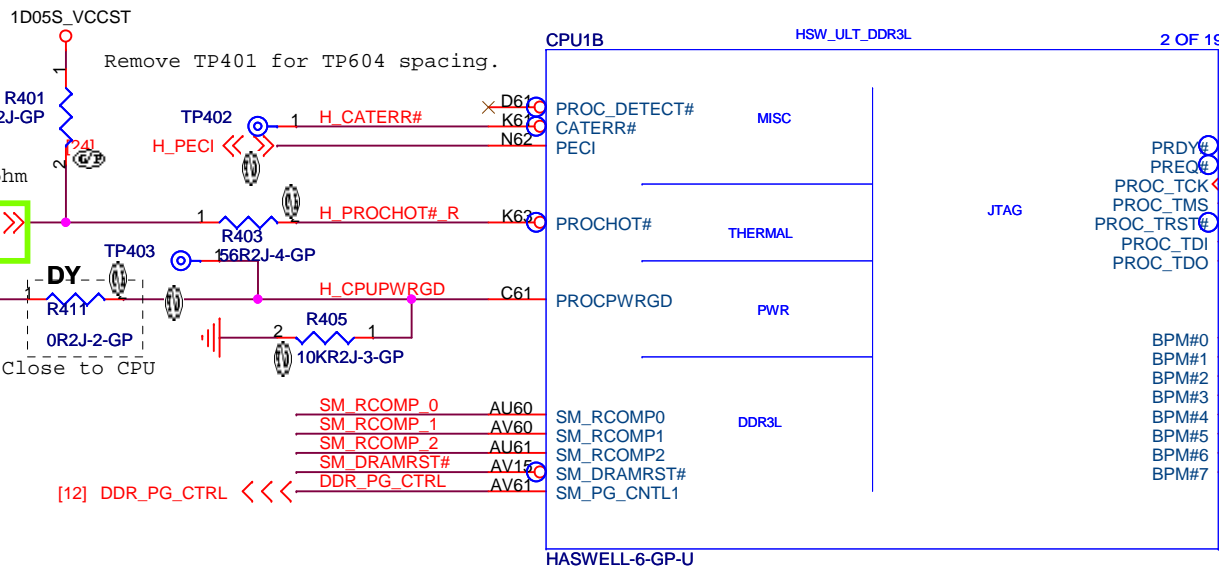
Layout Note: Close to CPU



Layout Note:

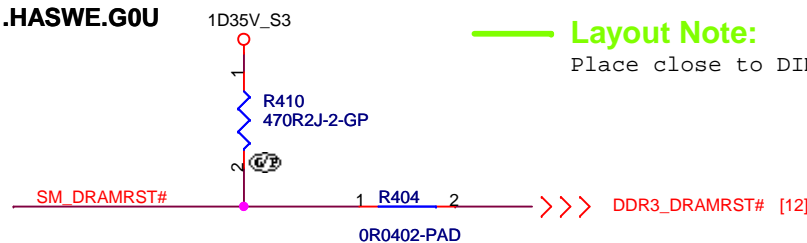
Design Guideline:

SM_RCOMP keep routing length less than 500 mils.



Layout Note:

Place close to DIMM



<Core Design>

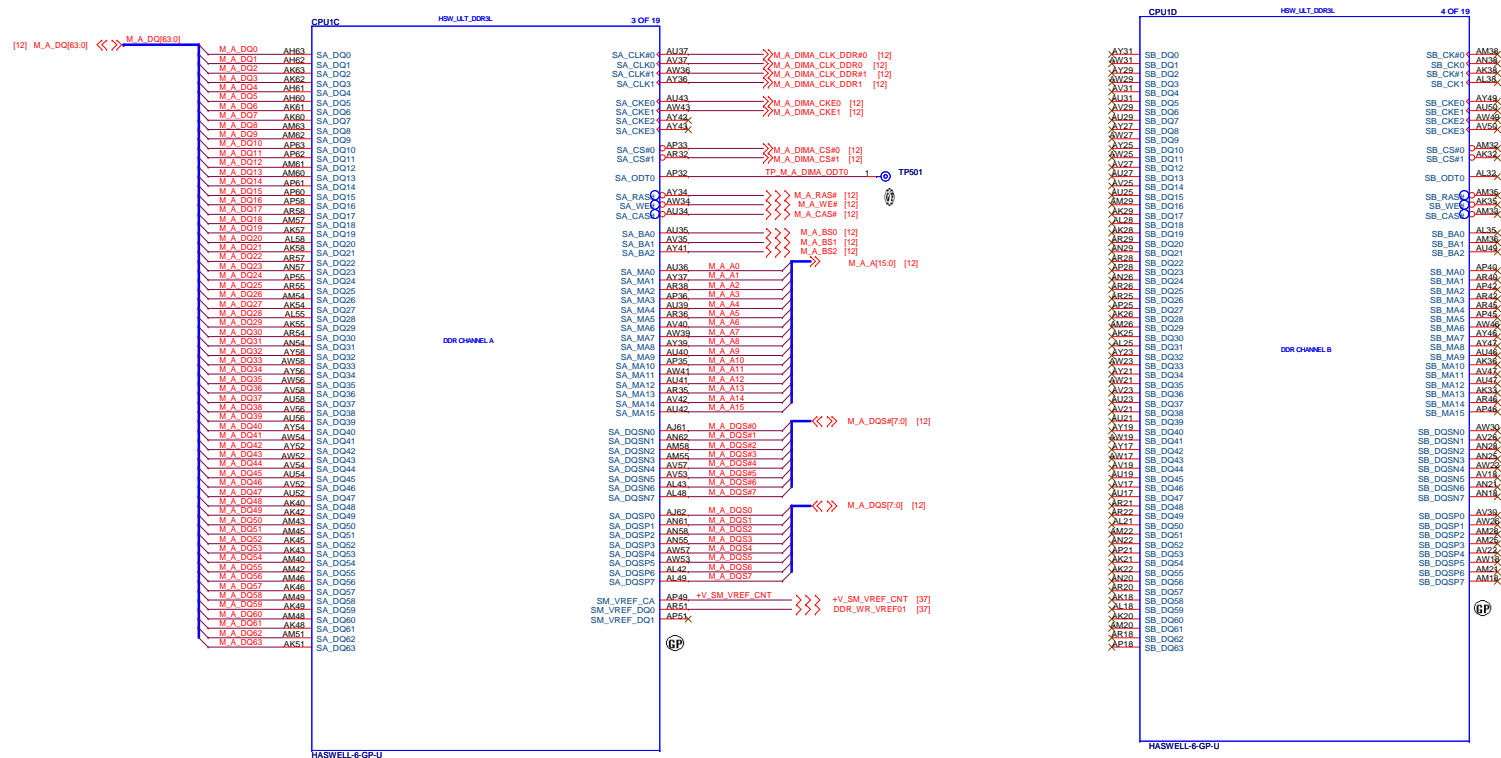


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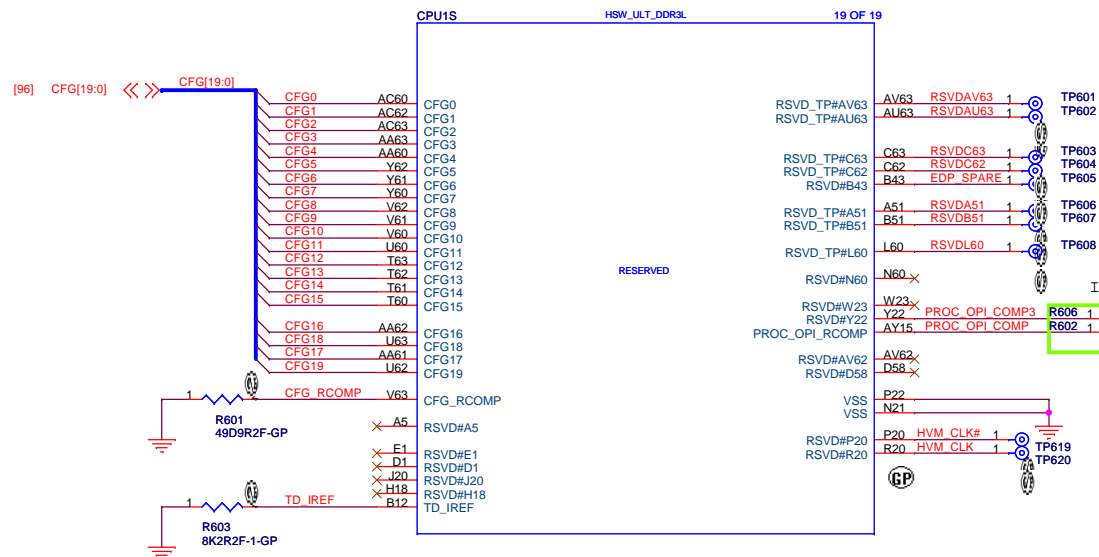
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Title		
CPU (THERMAL/MISC/PM)		
Size A4	Document Number Janus HSW 40/50/70	Rev A00
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DDR3L ball type: Non-Interleaved Type



SSID = CPU



7.4

Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left unconnected

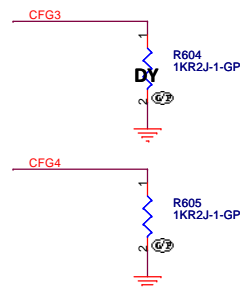
Intel Recommend

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"> • CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. • CFG[3]: MSR Privacy Bit Feature <ul style="list-style-type: none"> — 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting — 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • CFG[4]: eDP enable <ul style="list-style-type: none"> — 1 = Disabled — 0 = Enabled • CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lanes. 	I/O GTL



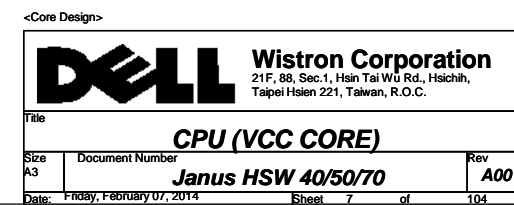
PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	<p>0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR</p> <p>1 : DISABLED</p>

DISPLAY PORT PRESENCE STRAP	
CFG[4]	<p>0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT</p> <p>1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT</p>

<Core Design>

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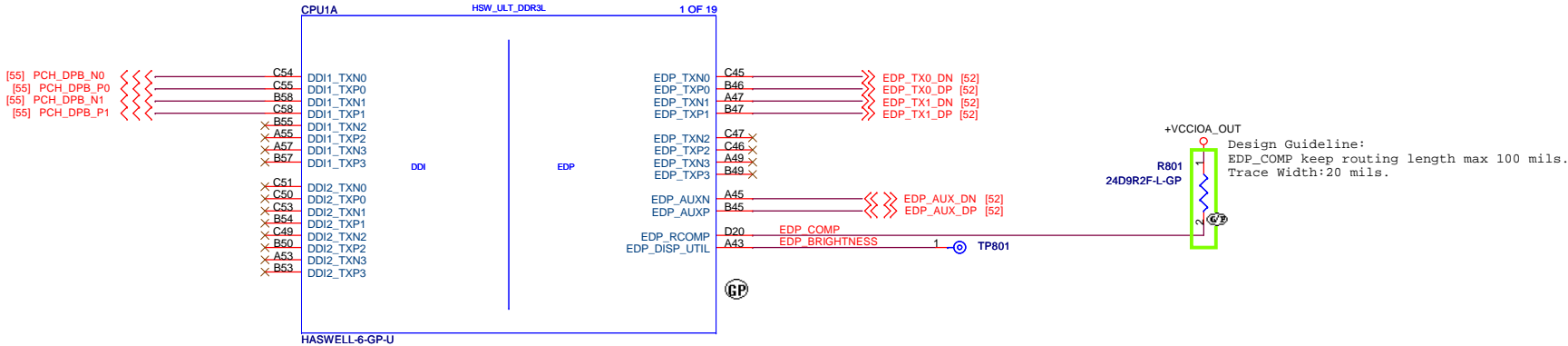
Title			CPU (CFG)
Size A3	Document Number	Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 6	of 104	



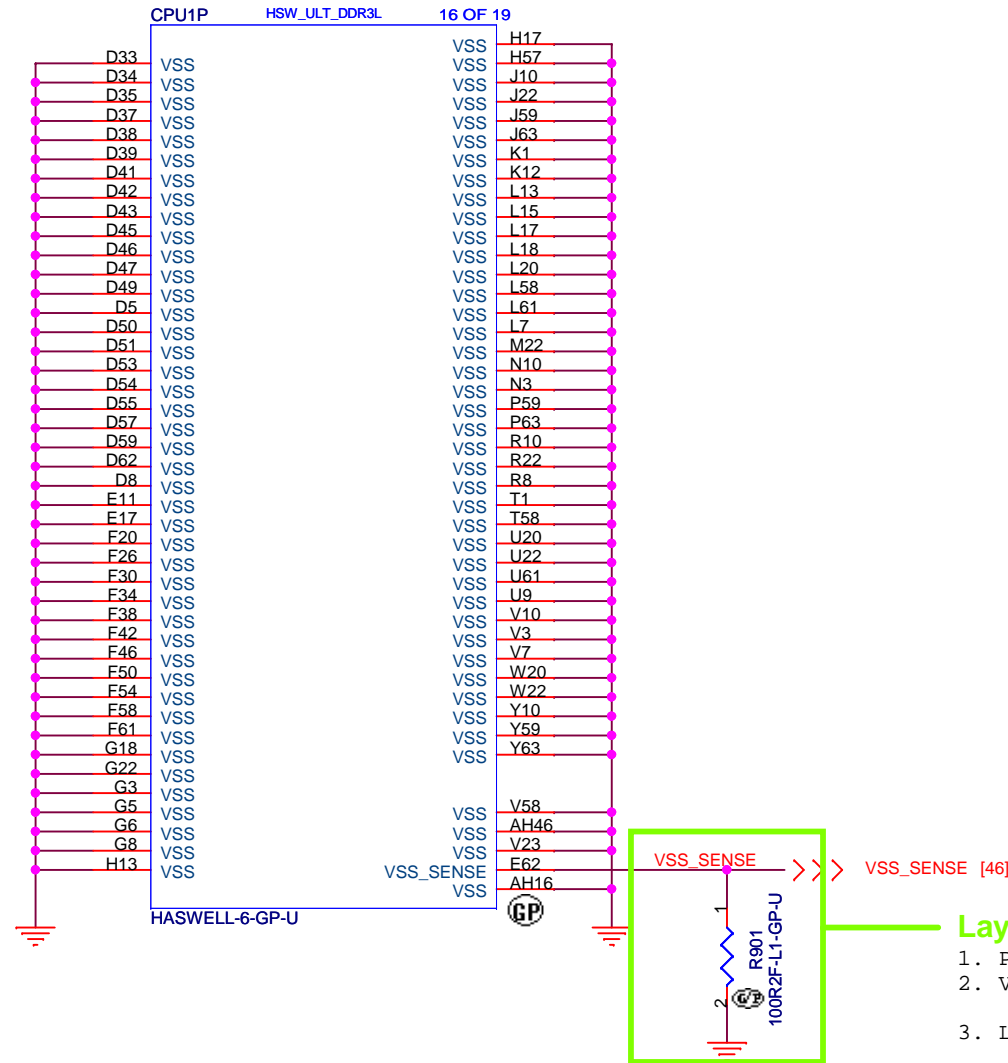
SSID = CPU

www.vinafix.vn

DP to VGA Converter



SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Title

CPU (VSS)

Size
A4

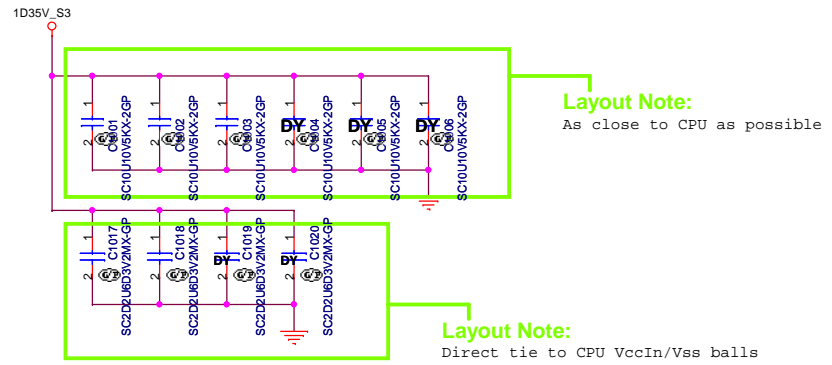
Document Number

Janus HSW 40/50/70

Rev
A00

Date: Friday, February 07, 2014

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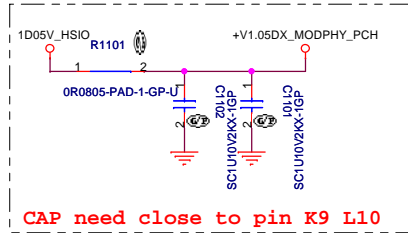


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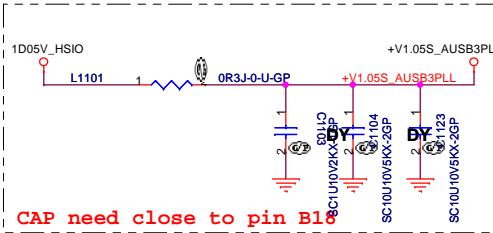
DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU (Power CAP1)		
Size A3	Document Number Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 10 of 104	

MAX: 1.92A

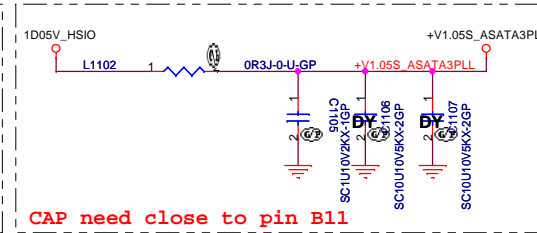
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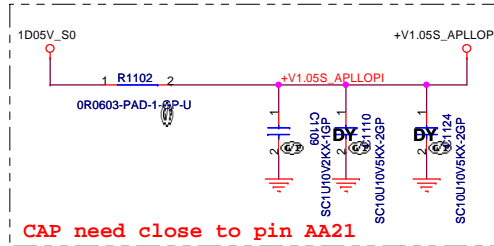
41mA



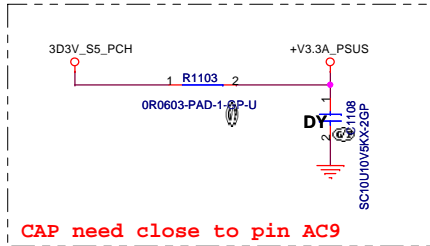
42mA



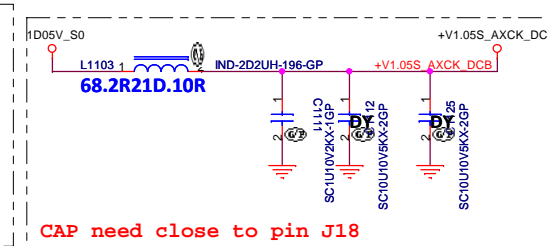
57mA



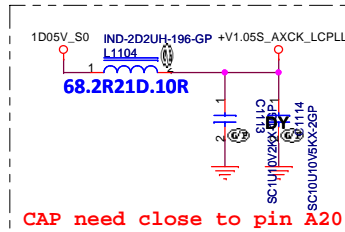
62mA



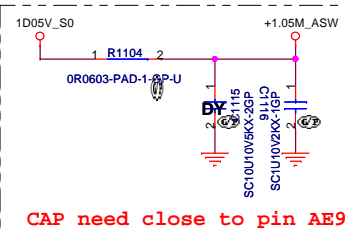
185mA



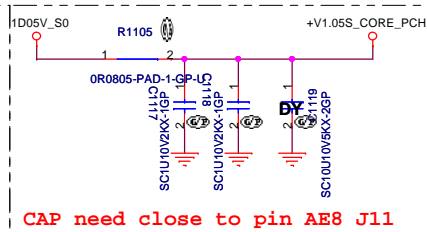
31mA



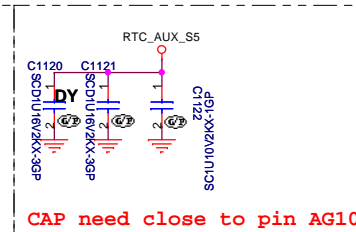
658mA



1.632A

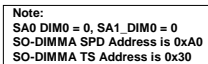


1mA



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title CPU (Power CAP2)	
Size A3	Document Number Janus HSW 40/50/70	Rev A00	
Date: Friday, February 07, 2014	Sheet 11 of 104		



Layout Note:
Place these Caps near SO-DIMMA.

O1201 must use $V_{th}=1V$.

Q1201
DMNFI 08K-3-CP

DWMNOL00K-7-GF

2

«Core Design:

B

1

Title

10

Size	Doc
A2	

Date:	Friday
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Title _____

DDR3-SODIMM1

Size	Document Number	Rev
A2	Issue HSW 10/E0/70	4

Date: Friday, February 07, 2014		Sheet 12 of 104	
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NAME	DATE	TIME	LOCATION	STATUS	REMARKS
1					

(Blanking)

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Title		
(Reserved)DDR3-SODIMM2		
Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00
Date: Friday, February 07, 2014	Sheet 13 of 104	

(Blanking)

<Core Design>



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Title
(Reserved)_SODIMM _SODIMM4

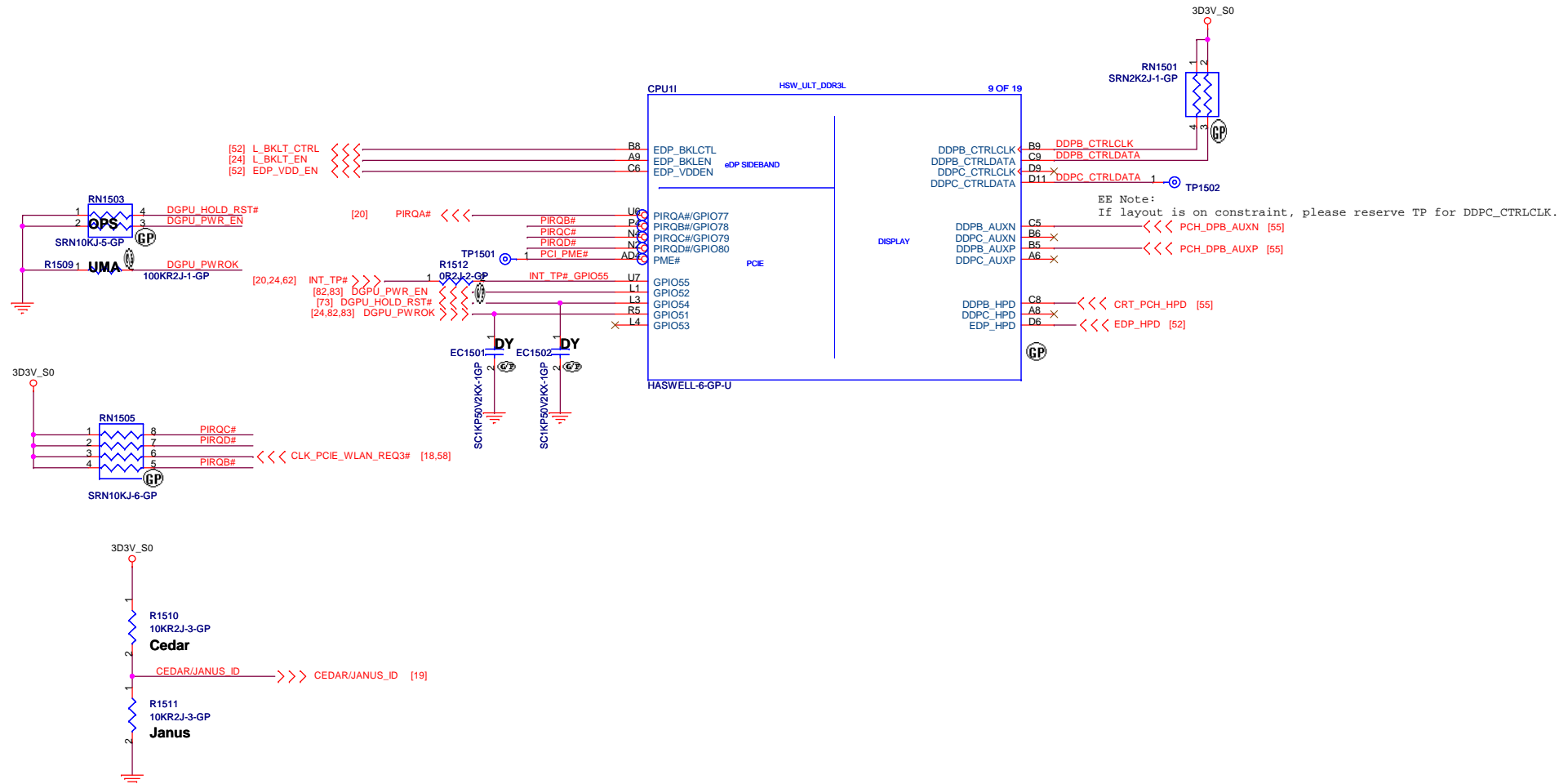
Size A4	Document Number Janus HSW 40/50/70	Rev A00
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Port B Detected

DDPC_CTRLDATA	* Low = Disable Port C (default) High = Enable Port C
----------------------	--

The internal pull-down is disabled after PLTRST# deasserts



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Title

PCH (EDP/GPIO/DDI)

Size

Document Number

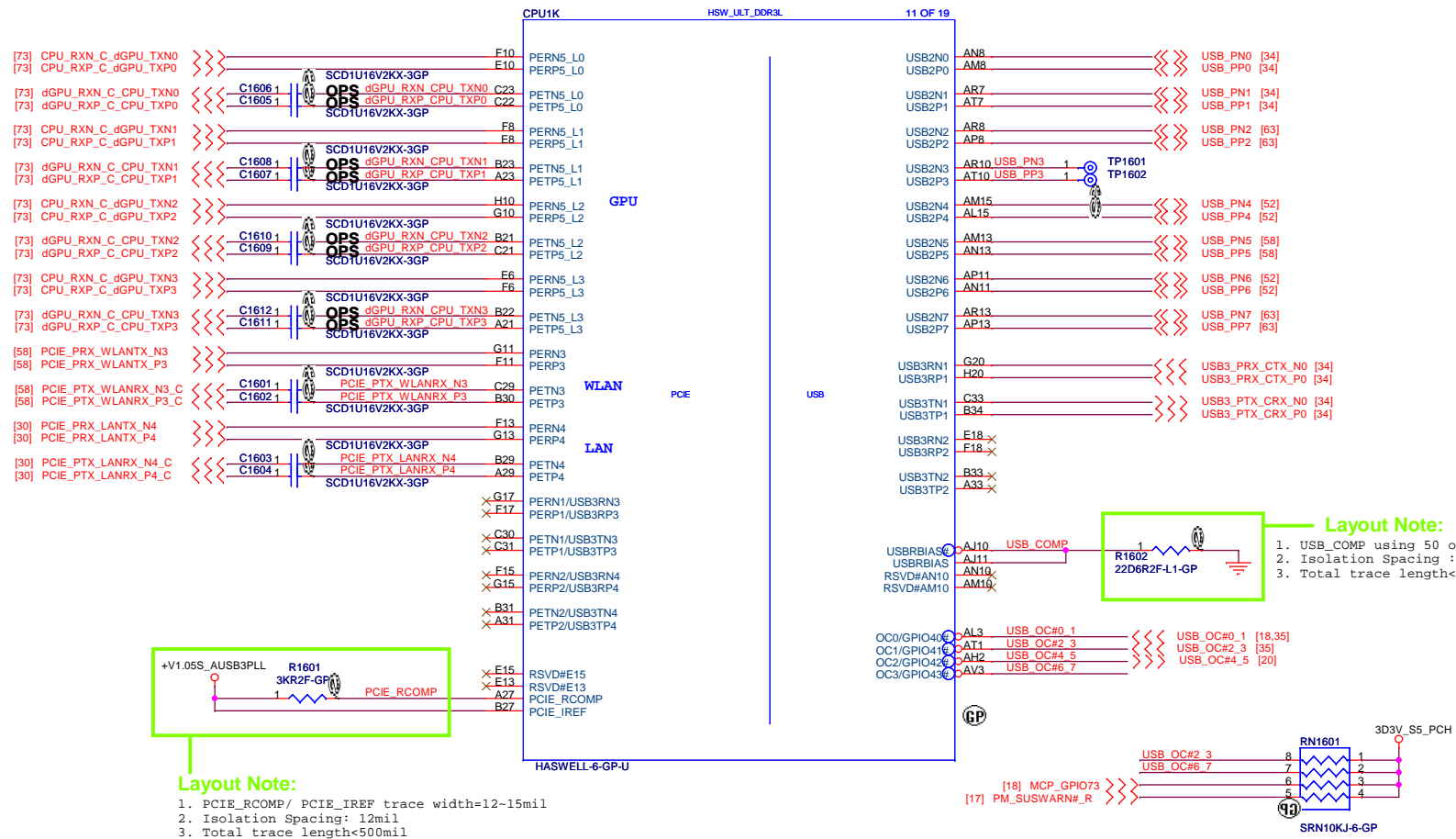
Janus HSW 40/50/70

Date _____

Friday, February 07, 2014

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SSID = PCH



PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5 (L0~L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU				

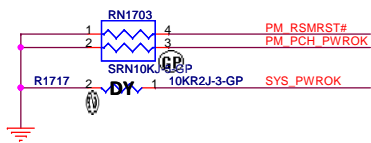
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Title			PCH (PCIE/USB)		
Size A3			Document Number		
Date: Friday, February 07, 2014			Rev A00		
Sheet 16 of 104			Janus HSW 40/50/70		

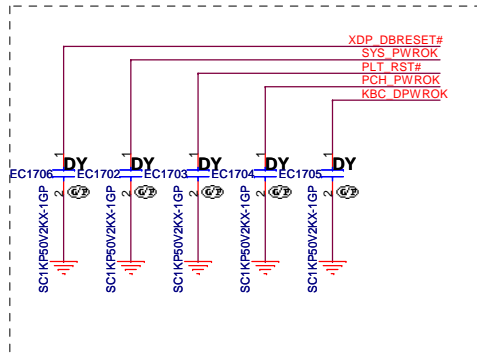
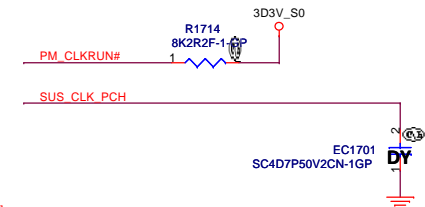
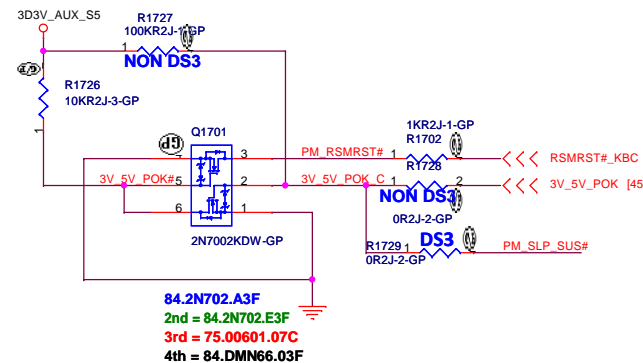
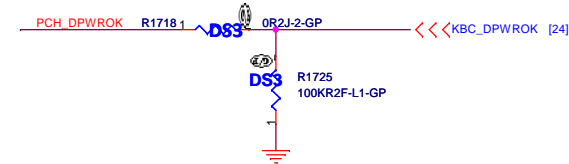
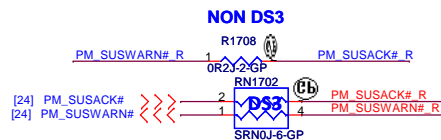
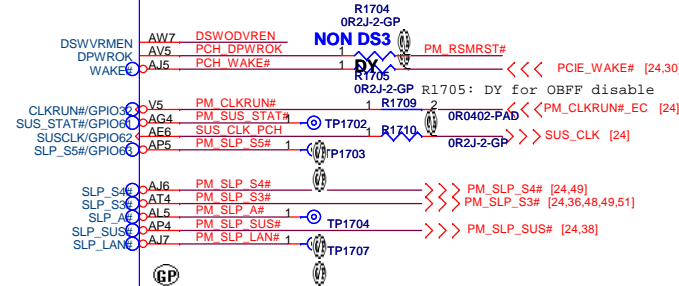
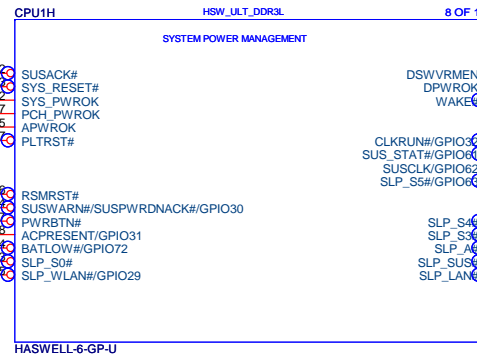
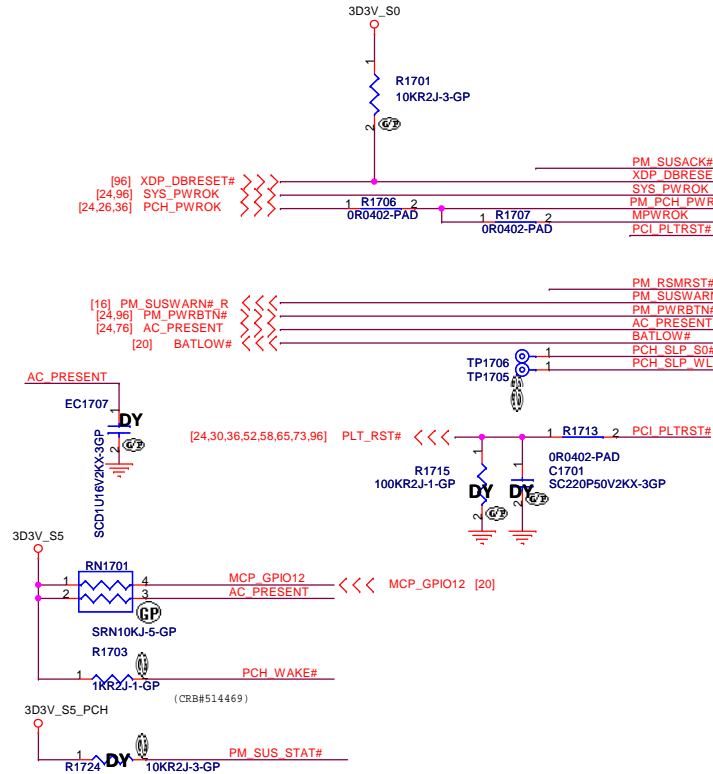
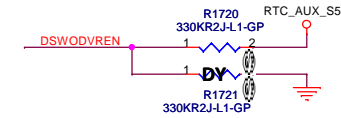
SSID = PCH



PCH strap pin:

On Die DSW VR Enable	
DSWVRMEN	Low = Disable High = Enable (default)

This signal has no integrated pull-up/pull-down.

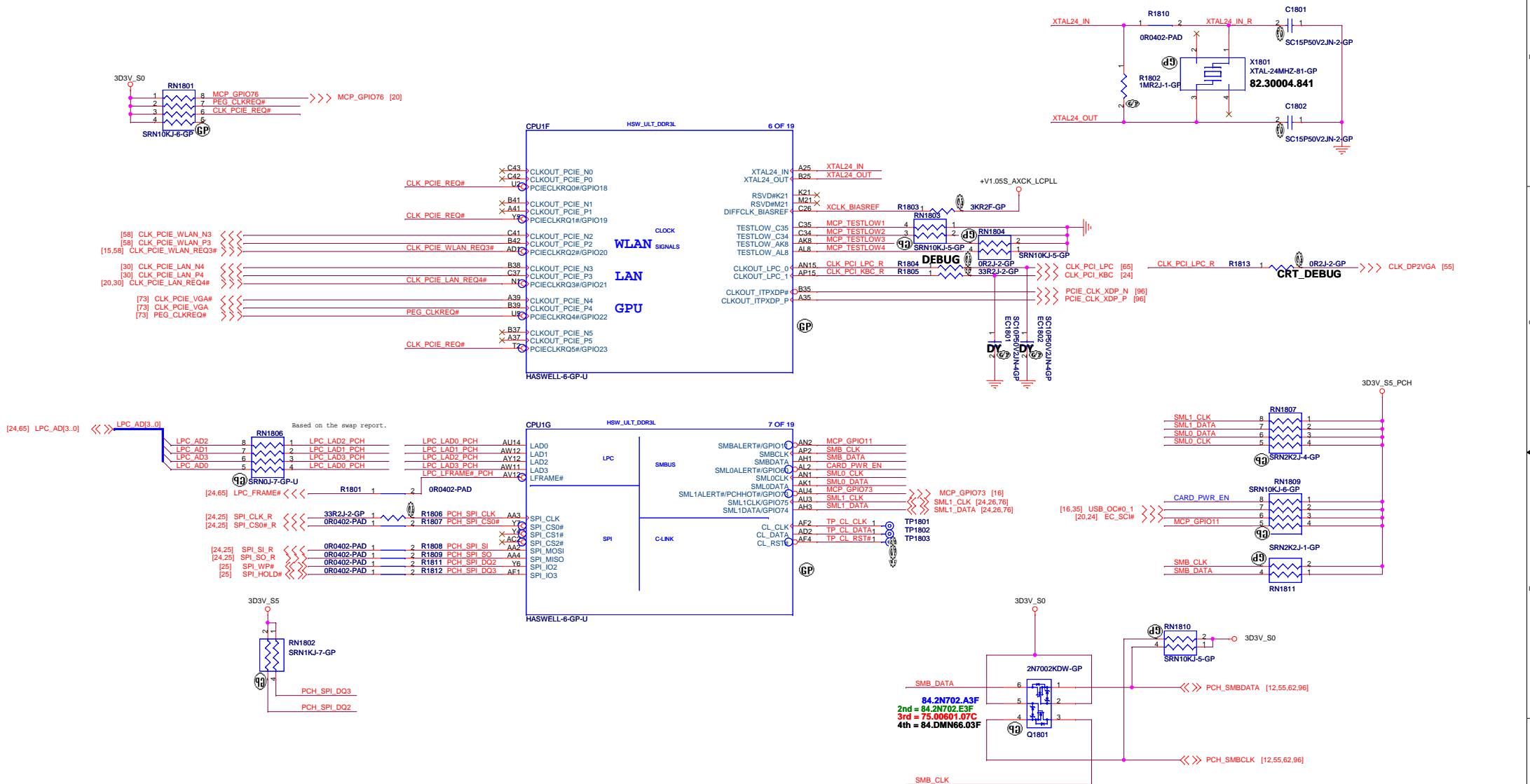


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Title			PCH (PM)	
Size	Document Number	Rev		
A3	Janus HSW 40/50/70	A00		
Date:	Friday, February 07, 2014	Sheet	17	of 104

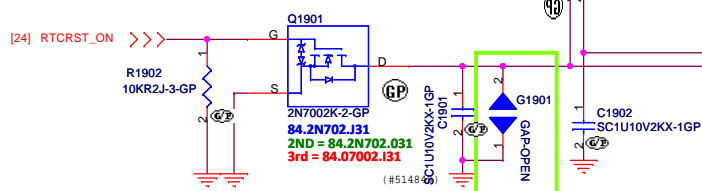
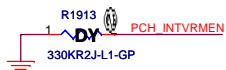
SSID = PCH



SS1D = CPU

PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

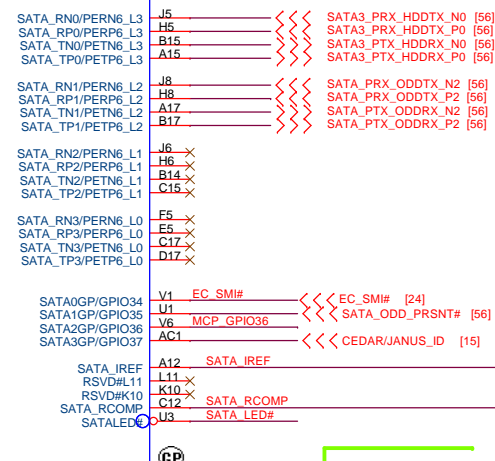
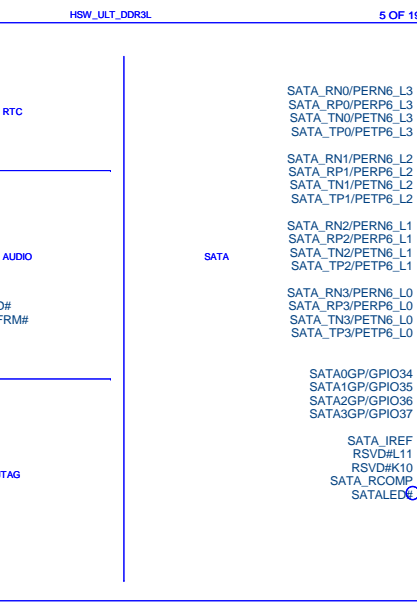
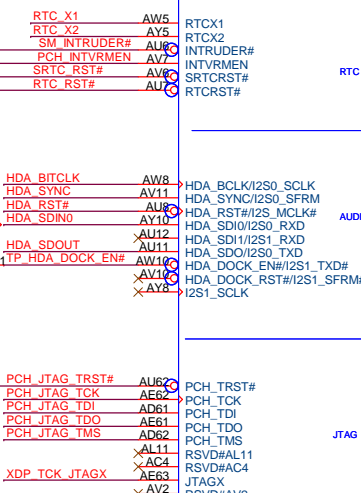
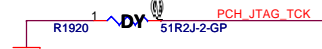
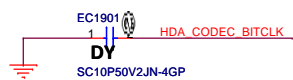
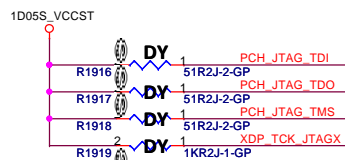
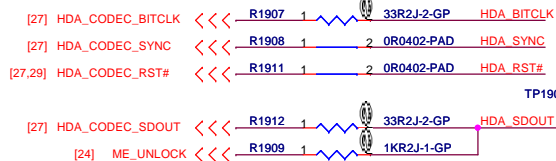


Layout: Place at the open door area.

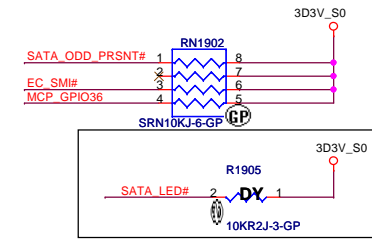
PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts



Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total <= 500mils.



Unused SATA[3:0]GP pins must be terminated to either 3.3V rail or GND using 8.2K to 10K on the motherboard. Either pull-up or pull-down is acceptable.

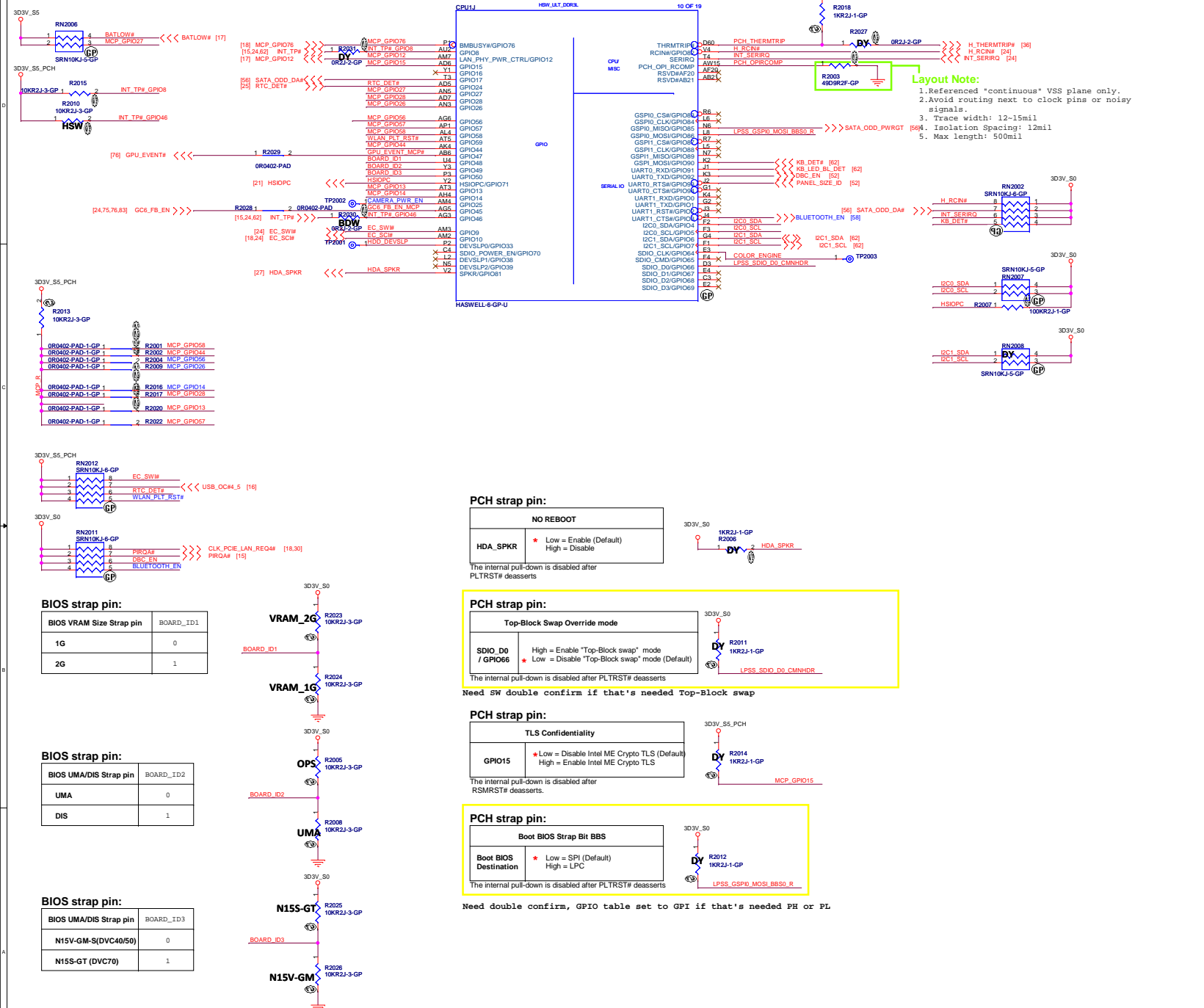
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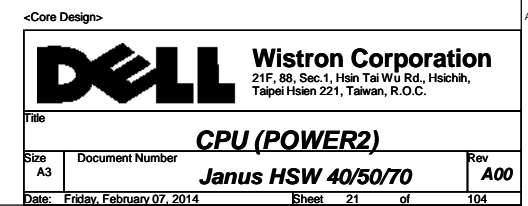
Title: **PCH (RTC/SATA/HDA/JTAG)**

Size: A3 Document Number: **Janus HSW 40/50/70** Rev: **A00**

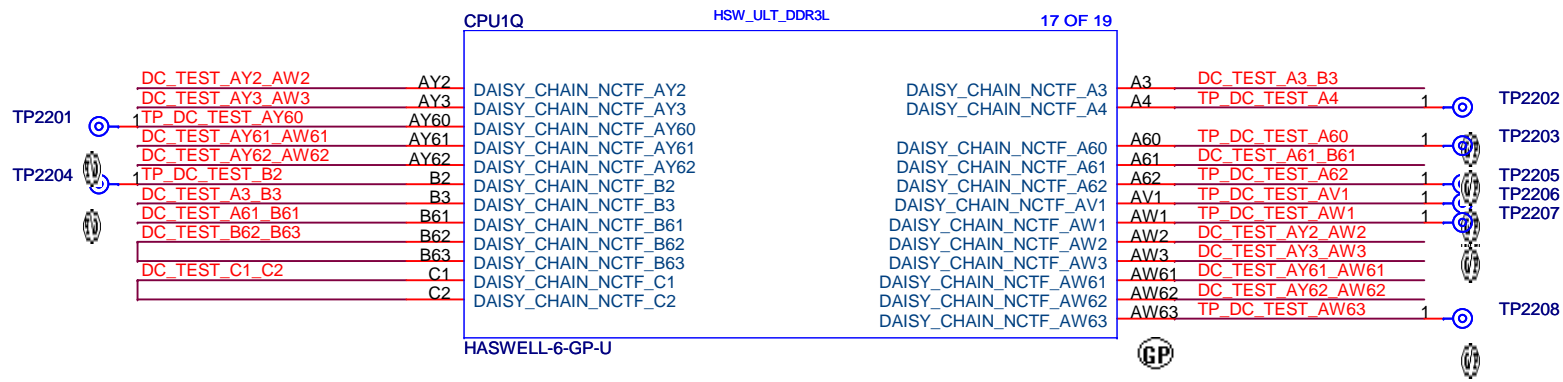
Date: Friday, February 07, 2014 Sheet: 19 of 104



<Core Design>



SSID = PCH



<Core Design>

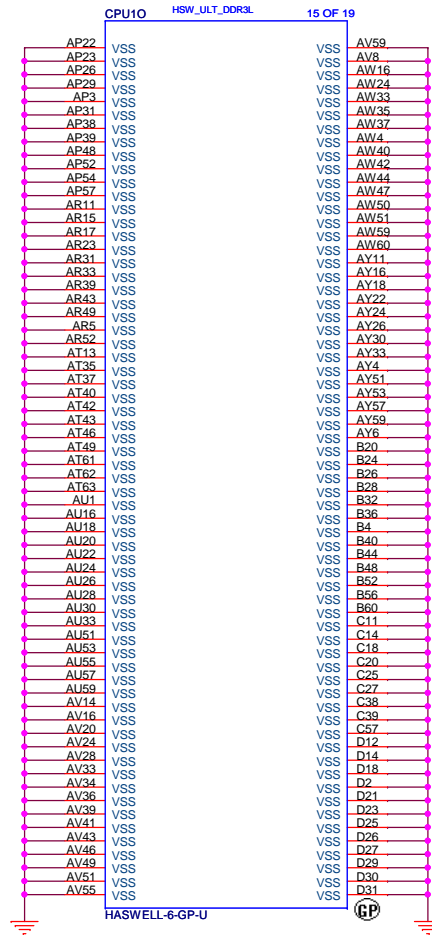
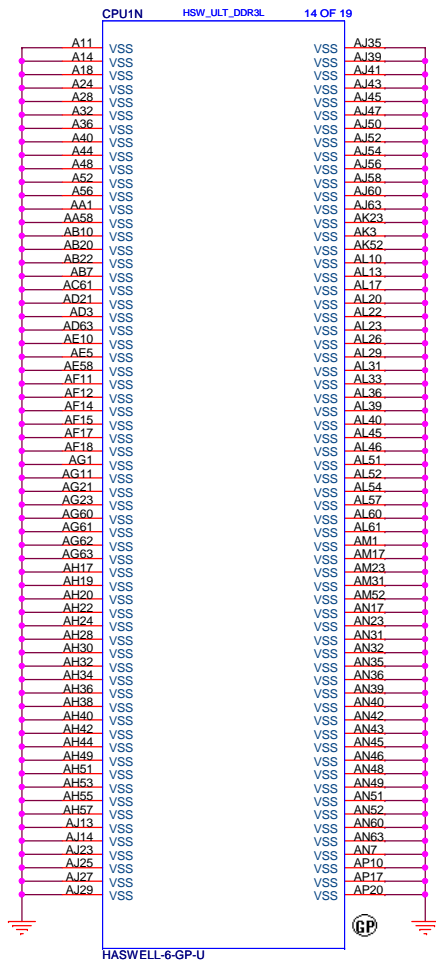
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Title
CPU (RSVD)

Size A4 Document Number **Janus HSW 40/50/70** Rev **A00**

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SSID = PCH



<Core Design>



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Title

CPU(VSS)Size
A3

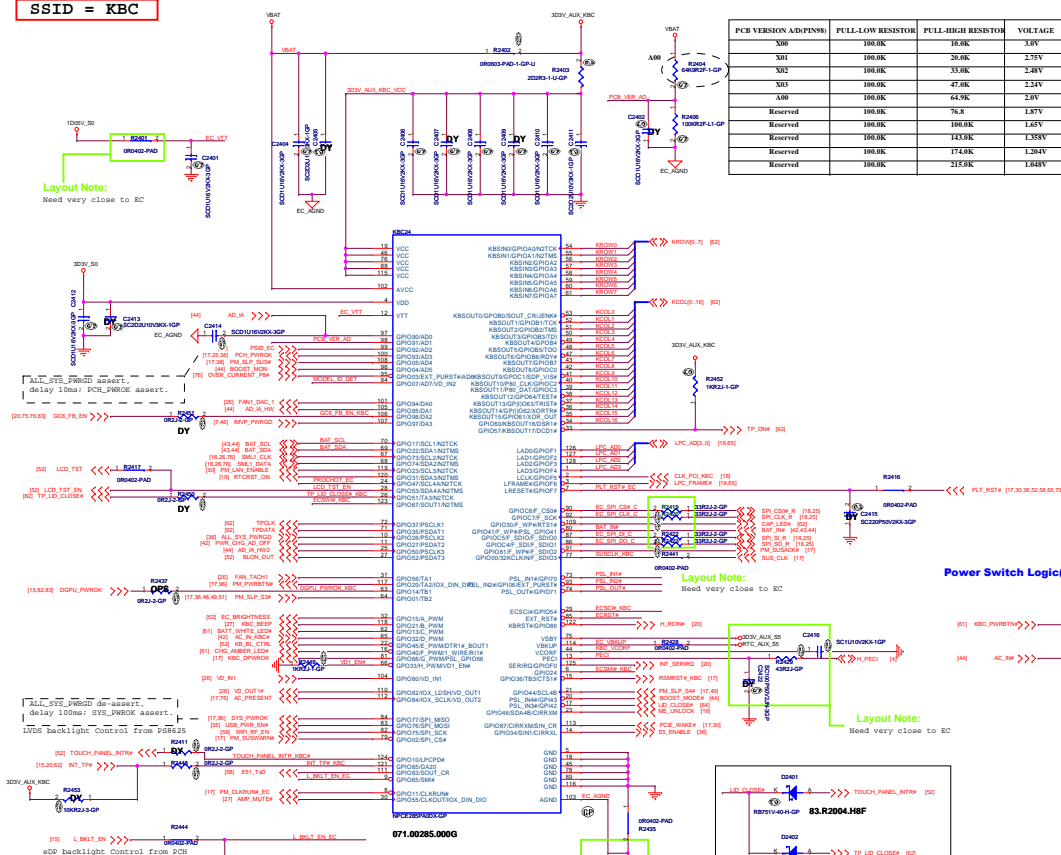
Document Number

Janus HSW 40/50/70Rev
A00

Date: Friday, February 07, 2014

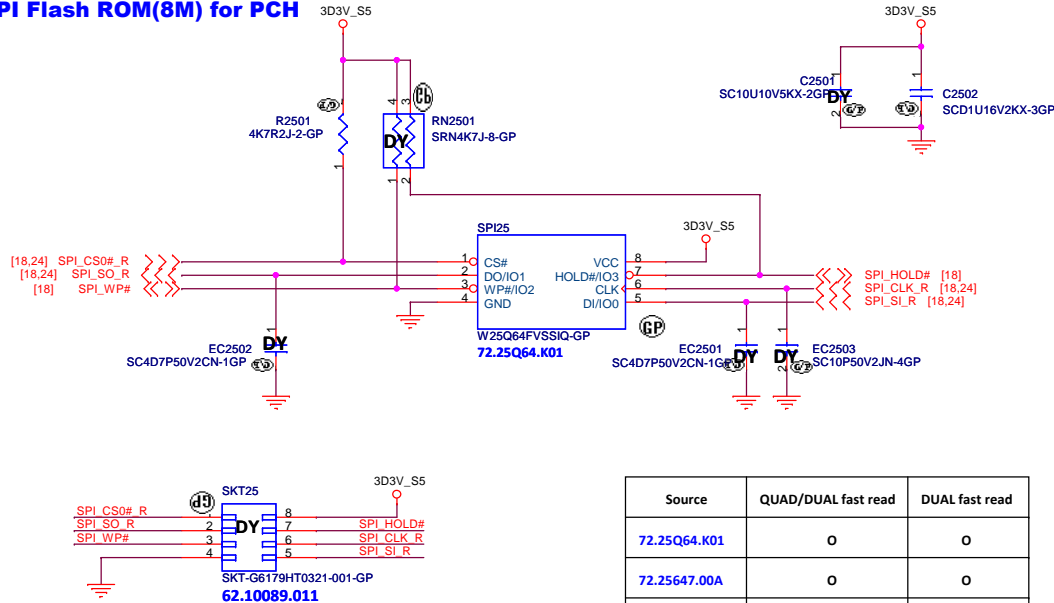
Sheet 23 of 104

SSID = KBC

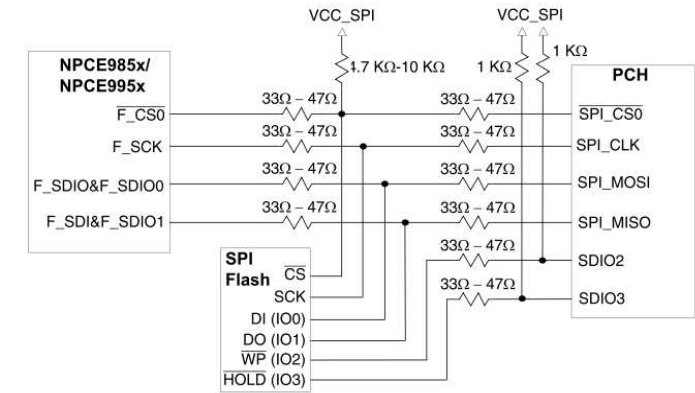


SSID = Flash.ROM

SPI Flash ROM(8M) for PCH

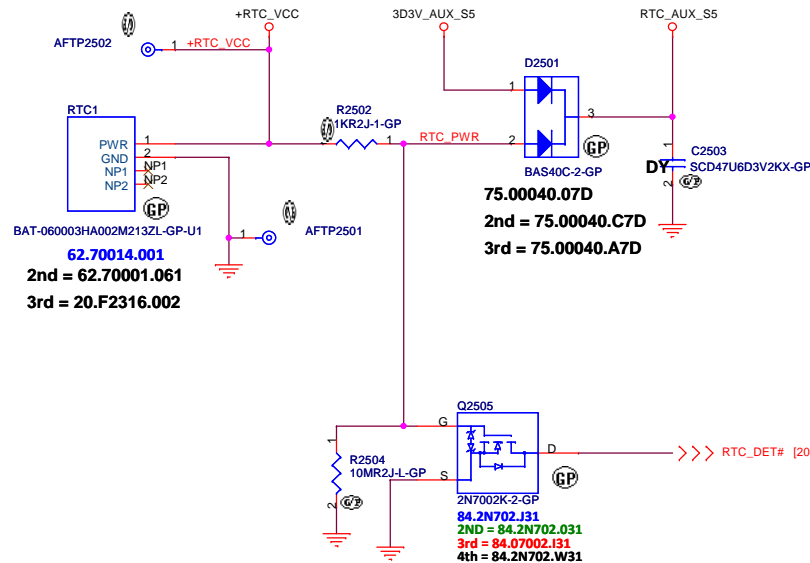


Single SPI shared flash connection (SPI Quad I/O mode)



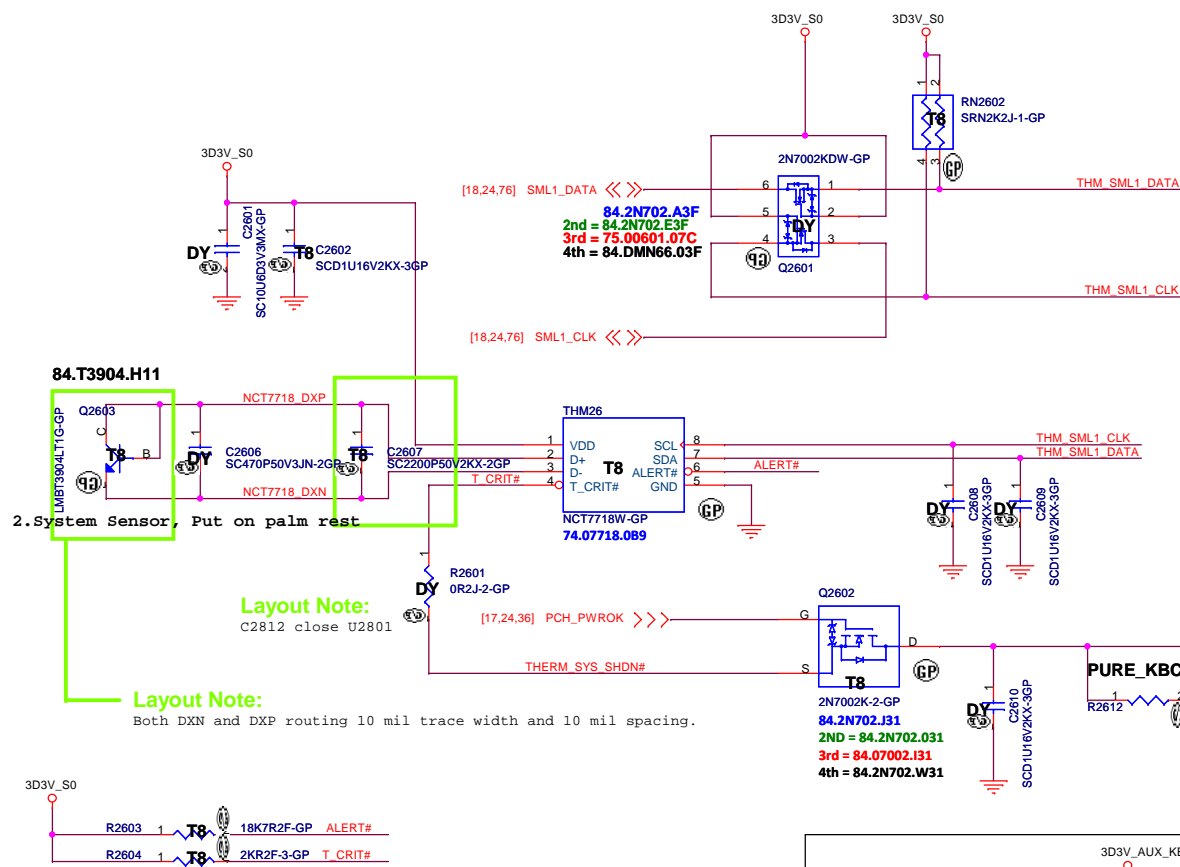
Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT

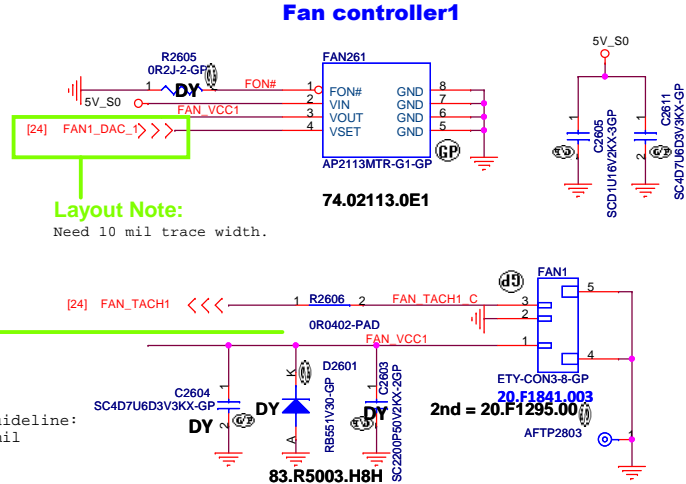
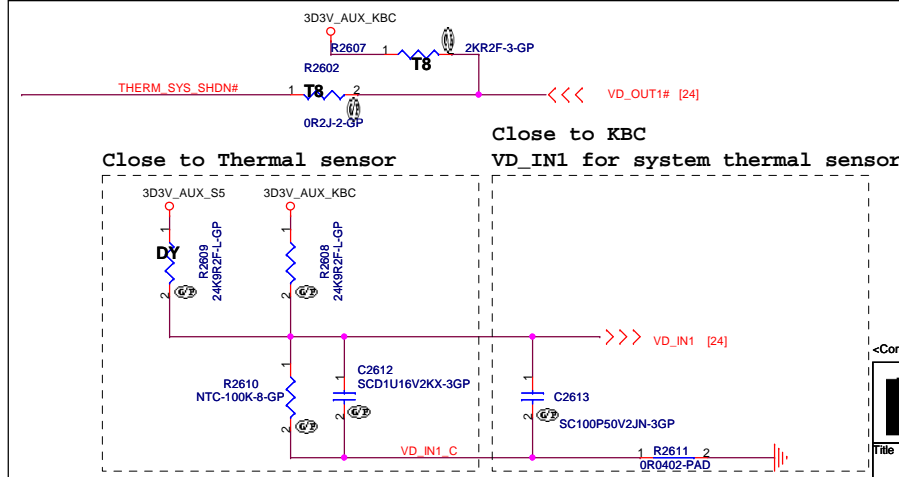


<Core Design>

SSID = Thermal



TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125





(Blanking)

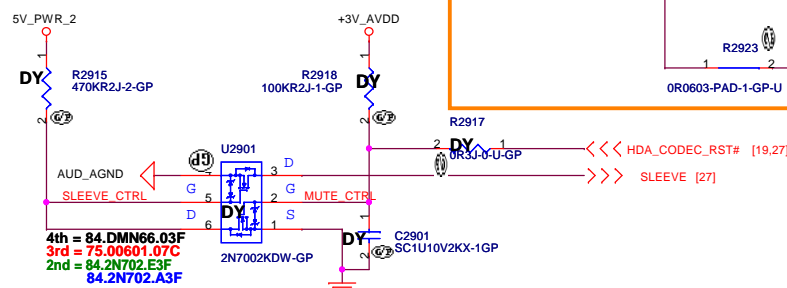
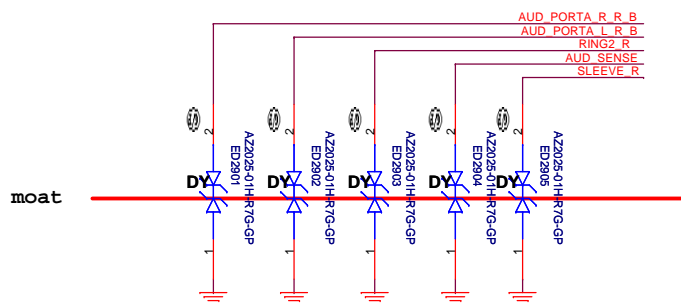
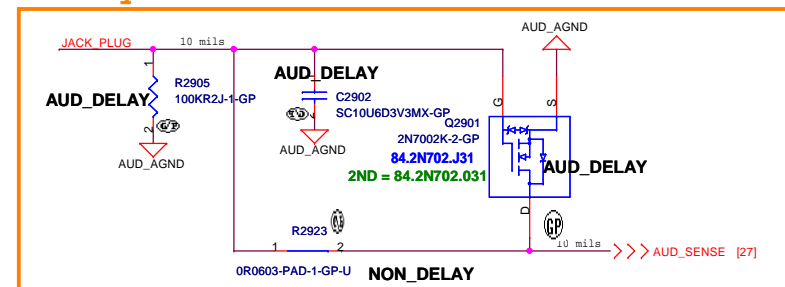
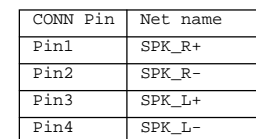
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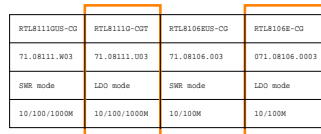
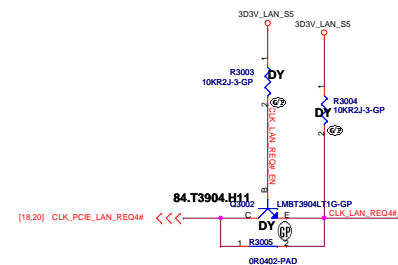
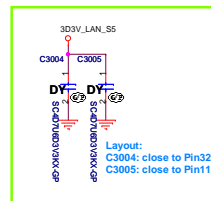
Title			Reserved		
Size	Document Number				Rev
A4	Janus HSW 40/50/70				A00
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Speaker trace width >40mil @ 2W4ohm speaker power

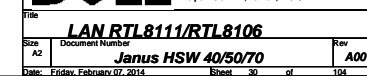


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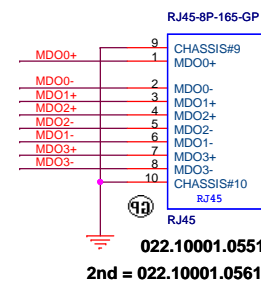
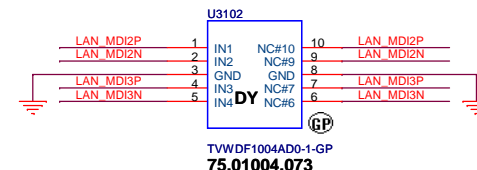
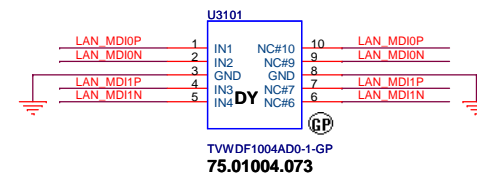
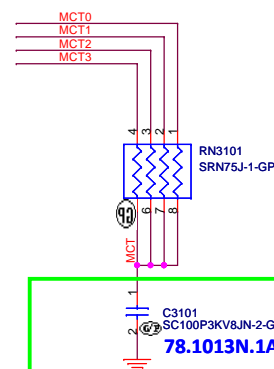
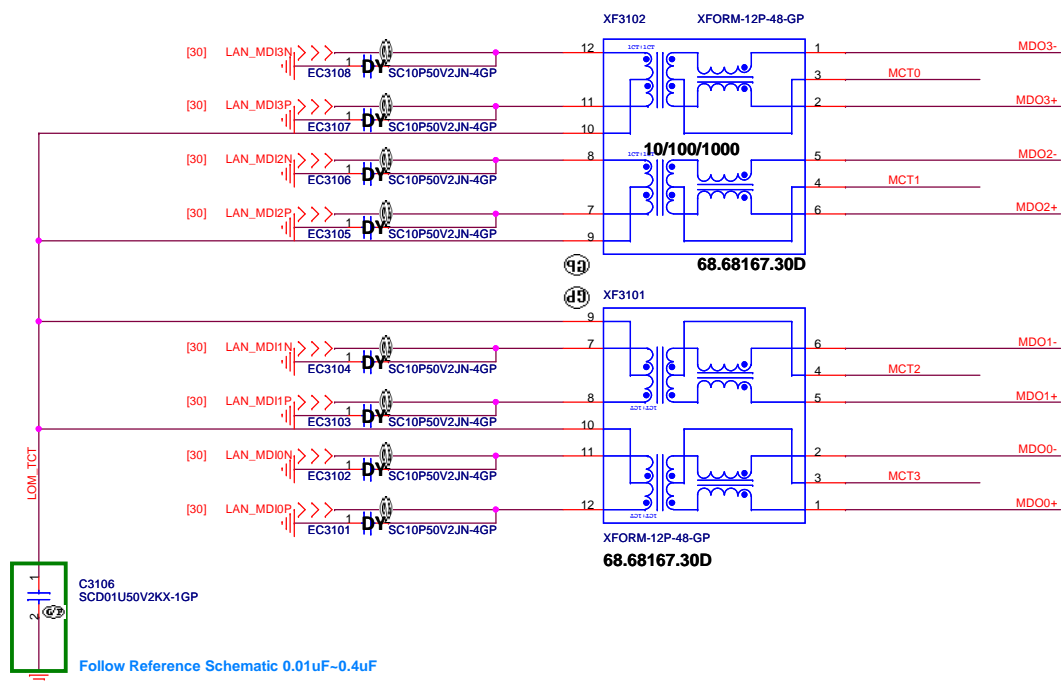
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Speaker/HPMIC			
Size A3	Document Number		Rev
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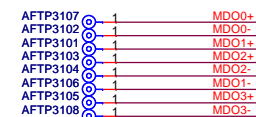
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Layout note:
30 mil spacing between MDI differential pairs.



Layout:
Place near RJ45



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<Core Design>



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Title		
(Reserved)Card Reader		
Size A4	Document Number Janus HSW 40/50/70	Rev A00
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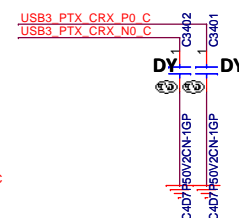
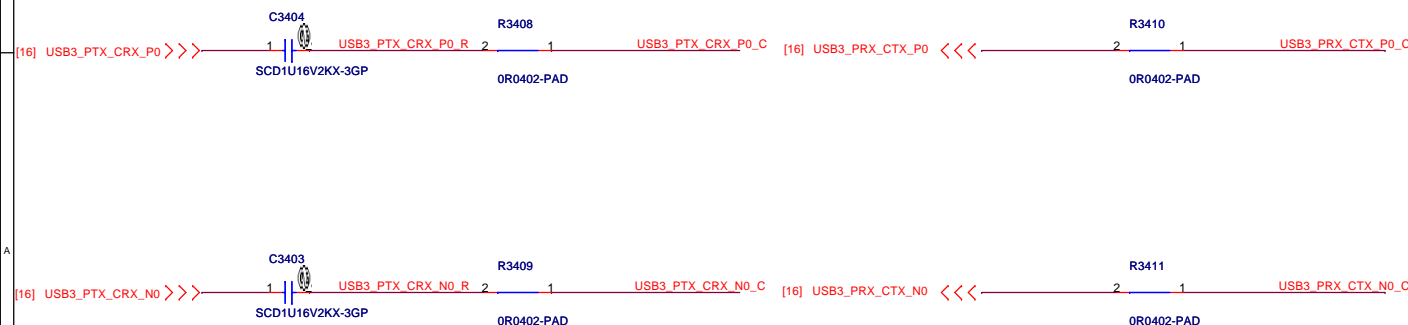
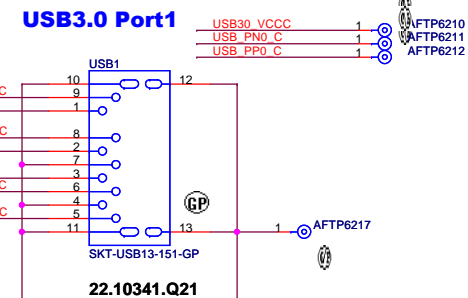
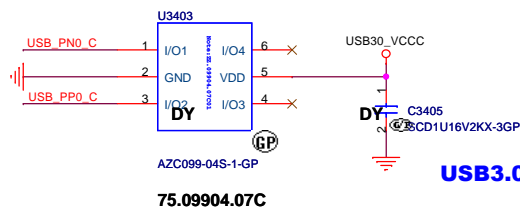
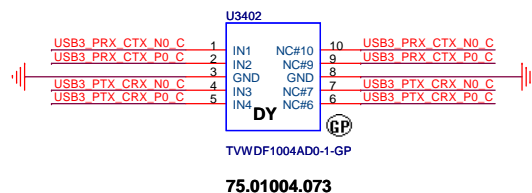
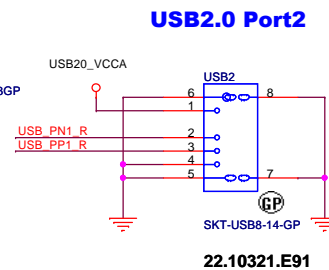
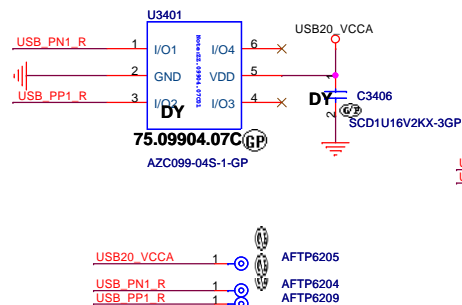
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Title		
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Size A4	Document Number Janus HSW 40/50/70	Rev A00
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SS1D = USB



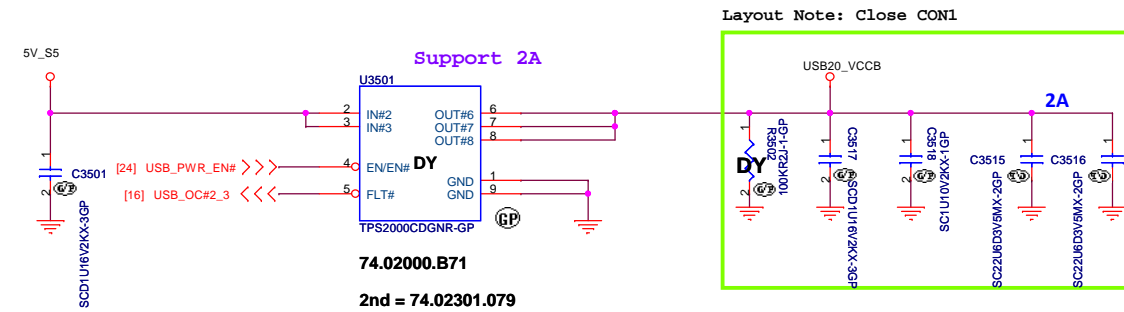
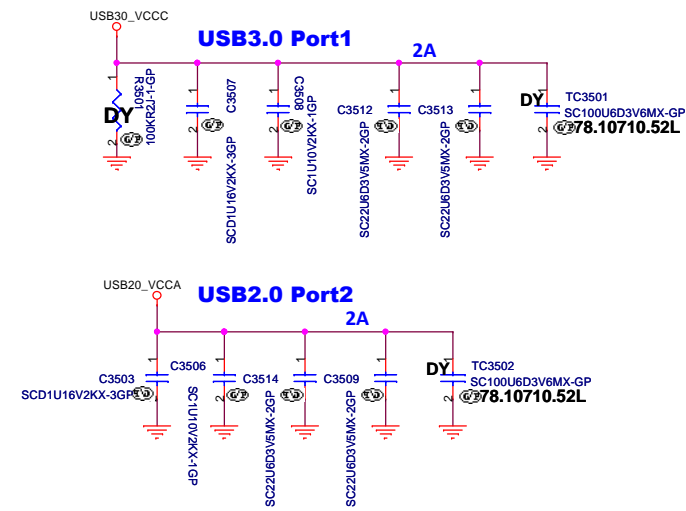
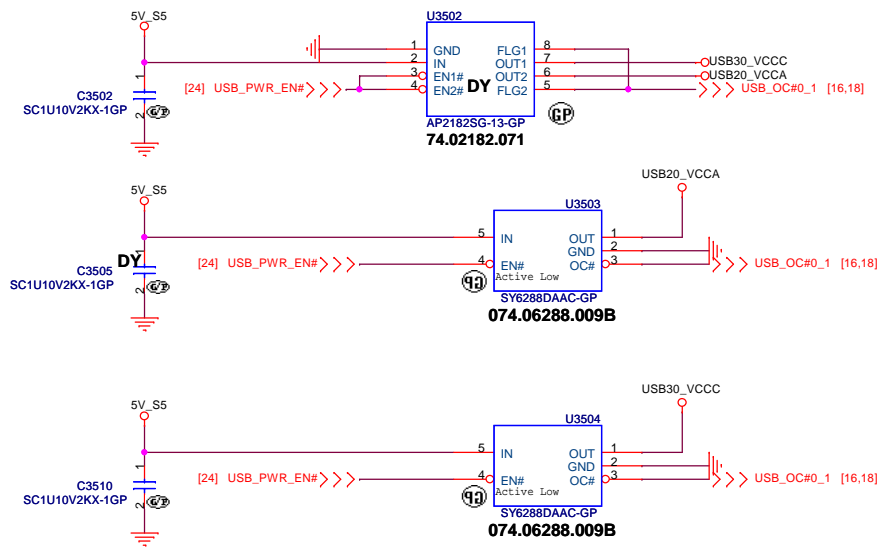
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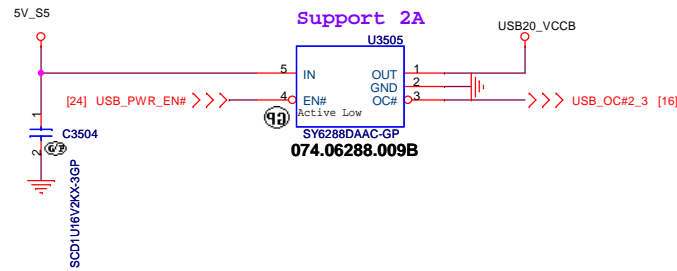
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Size: Custom Document Number: **Janus HSW 40/50/70** Rev: **A00**

Date: Monday, February 10, 2014 Sheet: 34 of 104



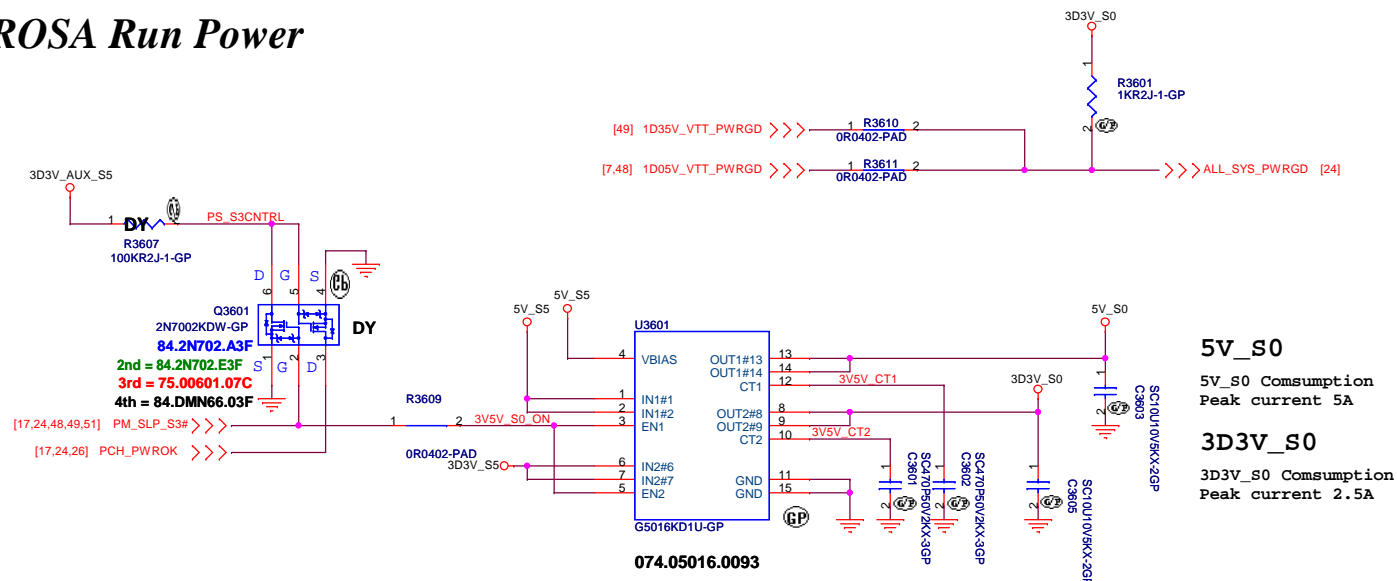
USB2.0 Port3 (IO Board)



<Core Design>

Power Good

ROSA Run Power

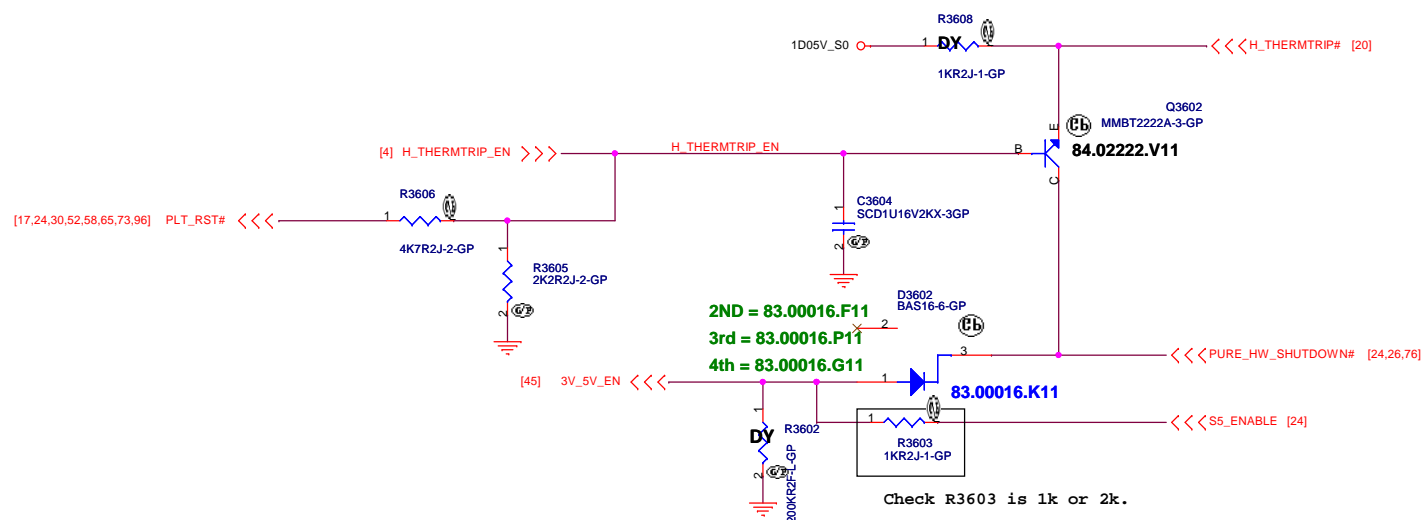


5V_S0

5V_S0 Consumption
Peak current 5A

3D3V_S0

3D3V_S0 Consumption
Peak current 2.5A



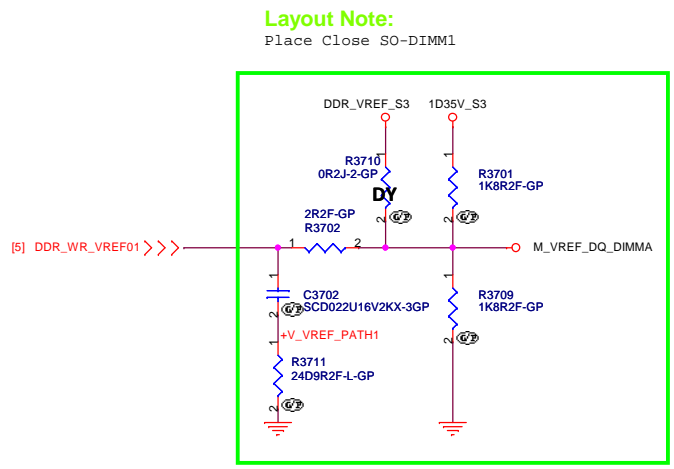
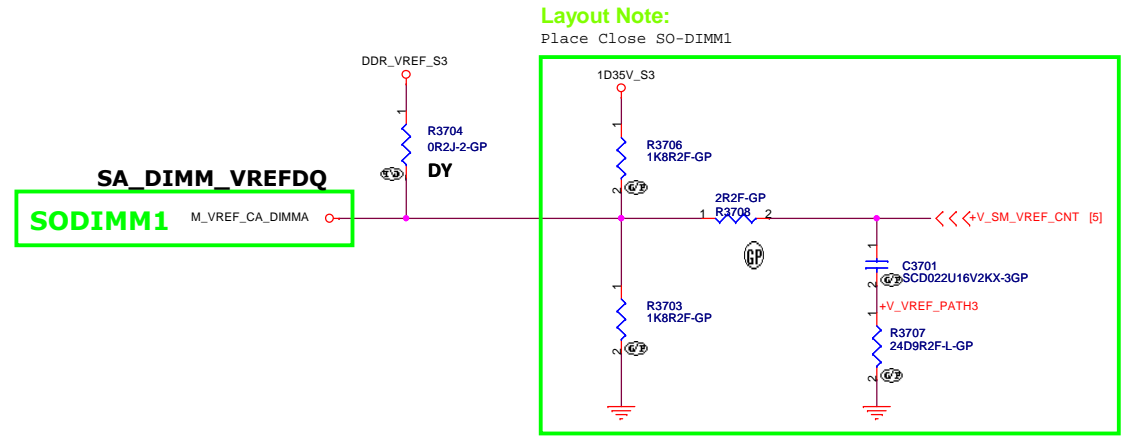
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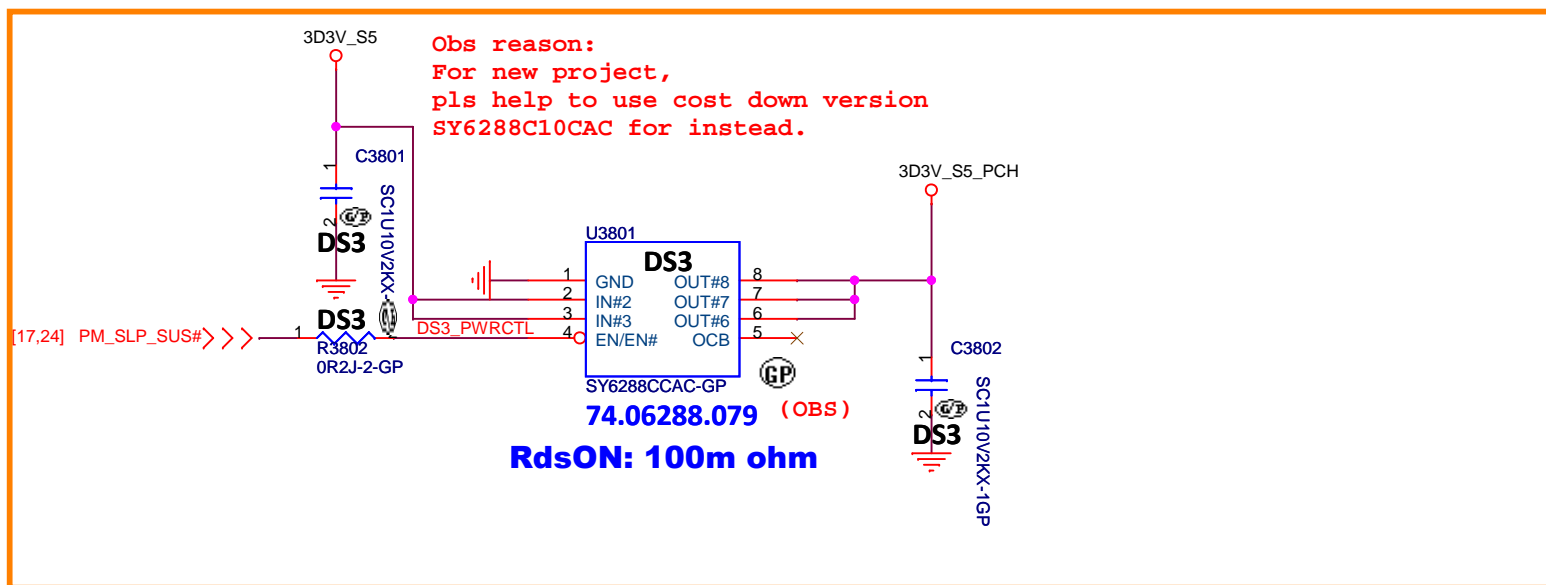


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Title			Power Plane Enable		
Size	Document Number		Rev		
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SSID = Reset.Suspend





Obs reason:
For new project,
pls help to use cost down version
SY6288C10CAC for instead.

<Core Design>



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Title

DSW

Size
A4

Document Number

Janus HSW 40/50/70

Rev
A00

Date: Friday, February 07, 2014

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Title
(Reserved) 1D05_M

Size A4	Document Number Janus HSW 40/50/70	Rev A00
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Date: Friday, February 07, 2014 Sheet 39 of 104

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Size
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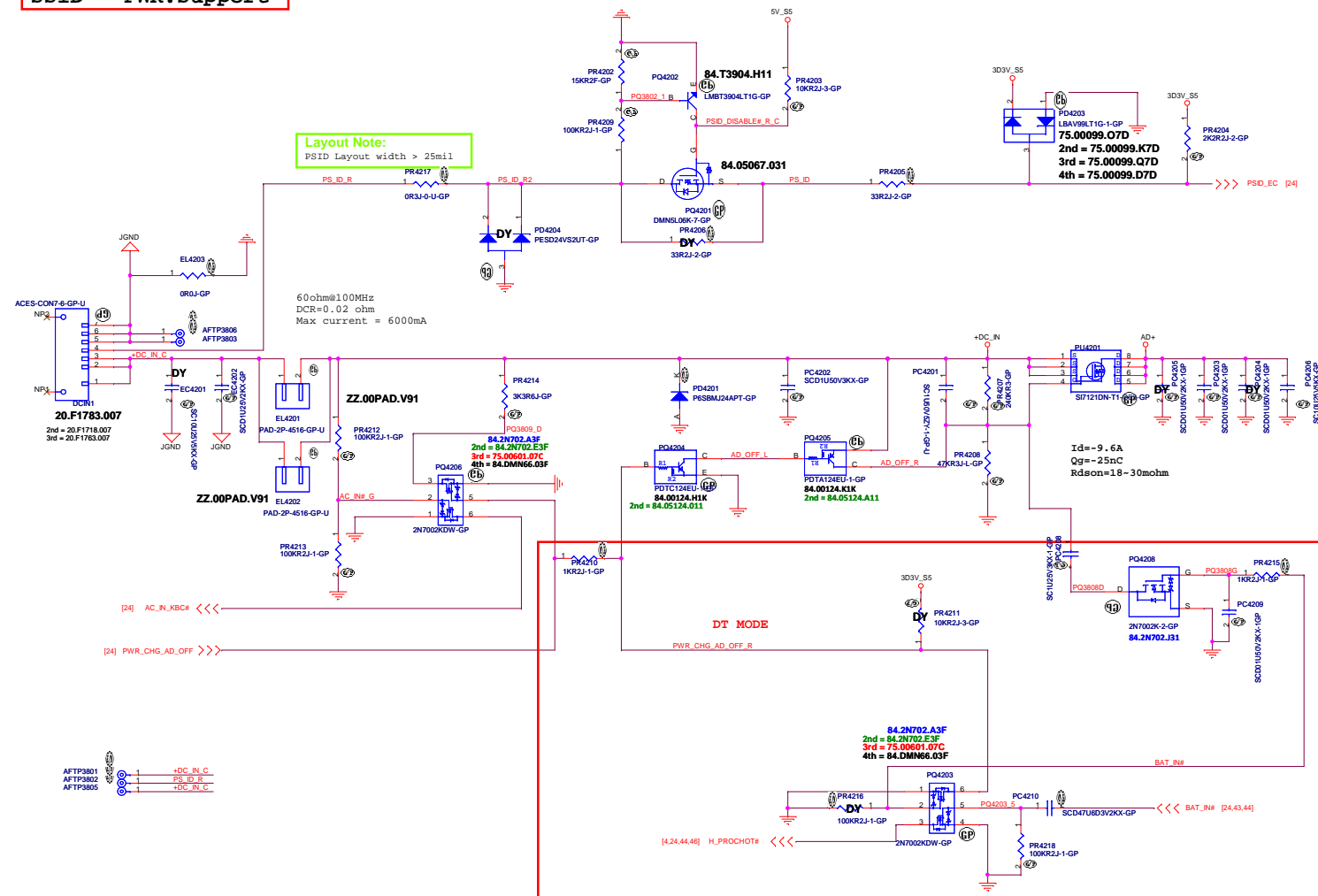
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Rev
A00

Date: Friday, February 07, 2014

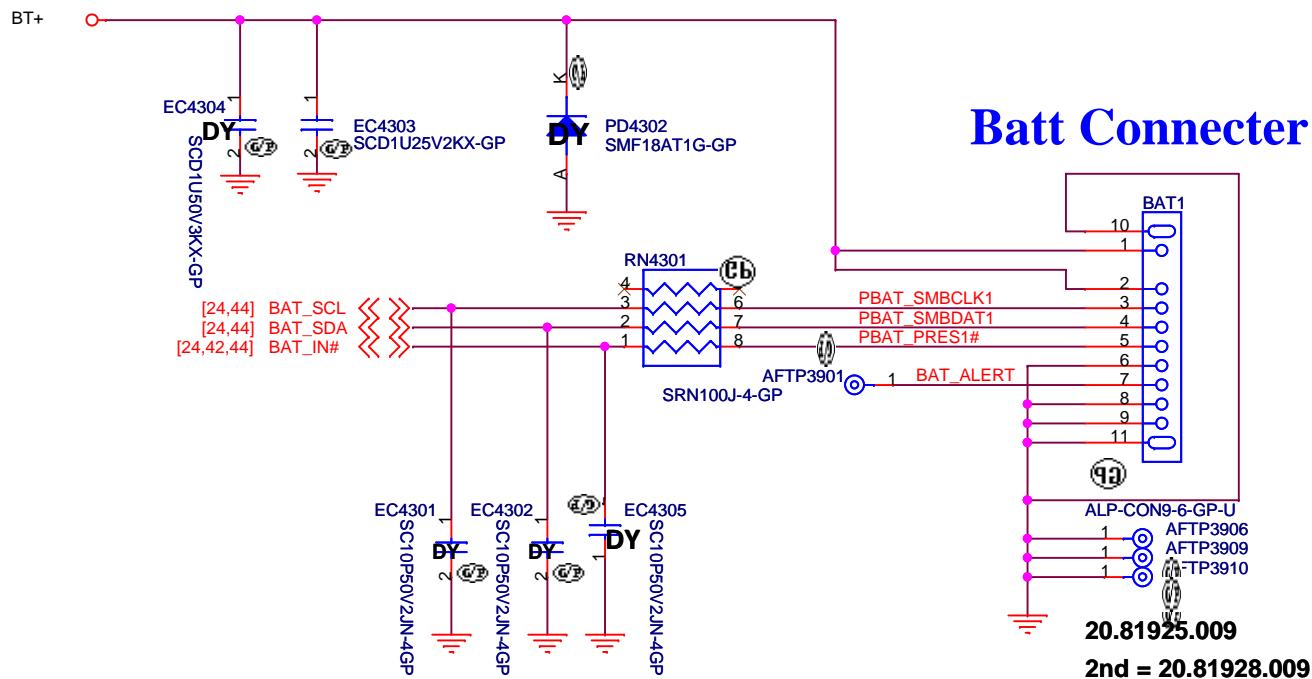
Sheet 41 of 104


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SSID = PWR.Support
```

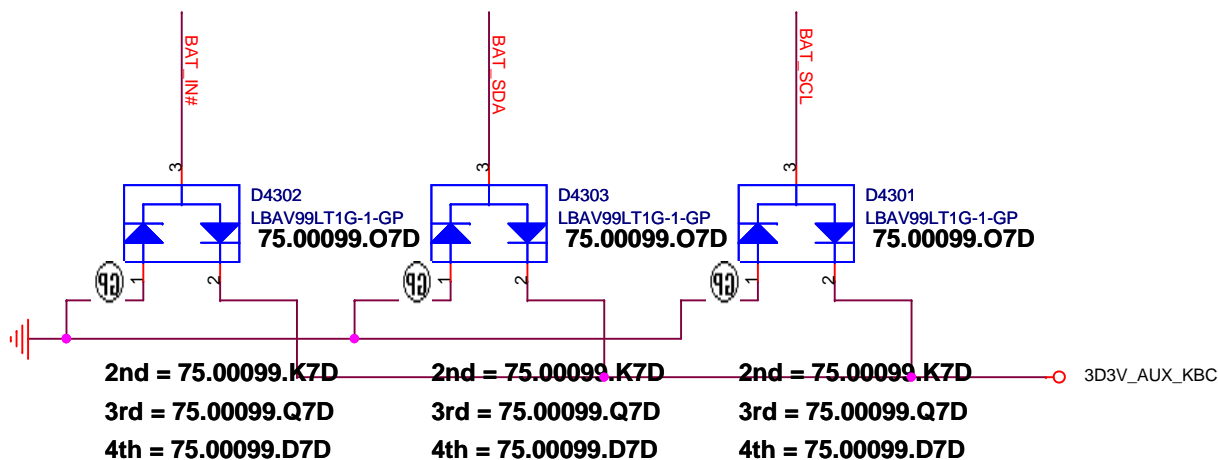


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SSID = PWR.Support



Placement: Close to Batt Connector



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Title

BATT CONN

Size
A4

Document Number

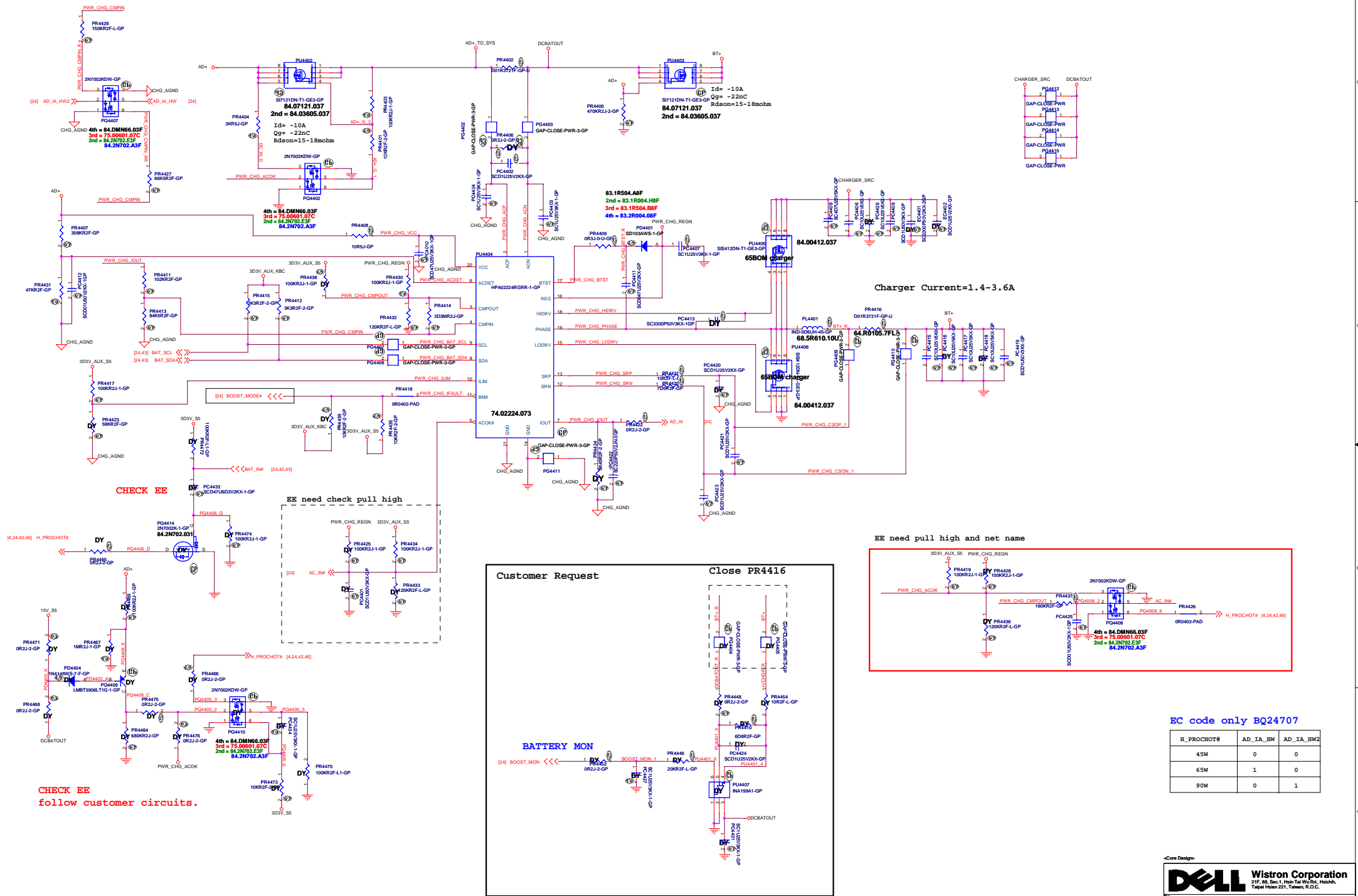
Janus HSW 40/50/70

Rev
A00

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SSID = Charger



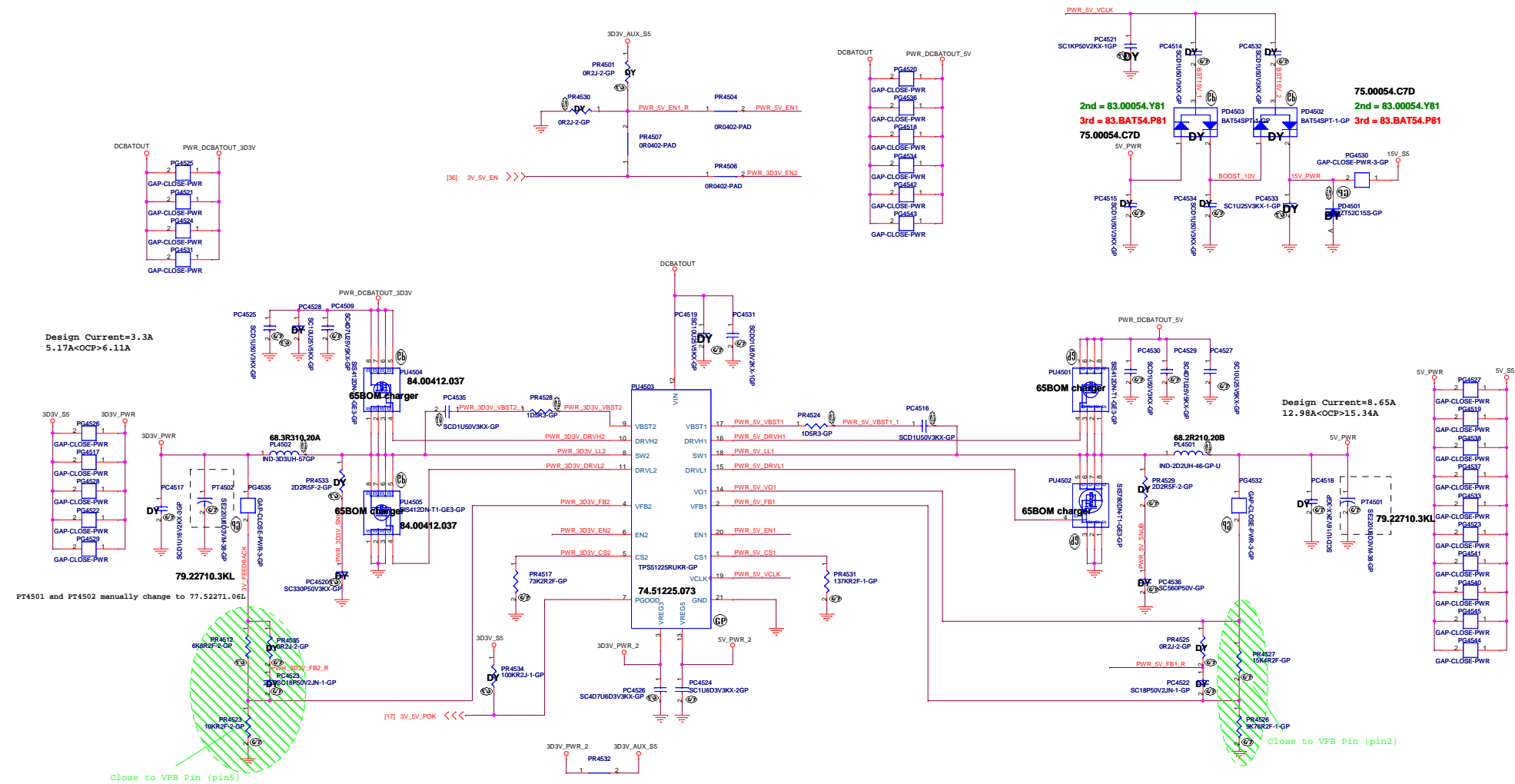
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File: **CHARGER HP402224**

Size: Document Number: **Janus HSW 405070**

Date: Friday, February 07, 2014 Rev: 44 of 154

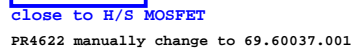


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP POL 220U 6.3V 4.6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SI5412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037
L/S:SI5780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U CMC637-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mhm / 77.52271.09L
H/S:SI5412 / 24.0mhm/30.0mhm4.5Vsg / 84.00412.037
L/S:SI5780 / 14.5mOhm/17.5mOhm4.5Vsg / 84.00780.037



	PR4603	PR4614
15W	1.27K 64.12715.6DL	90.9K 64.90925.6DL
28W	1.58K 64.15815.6DL	113K 64.11335.6DL

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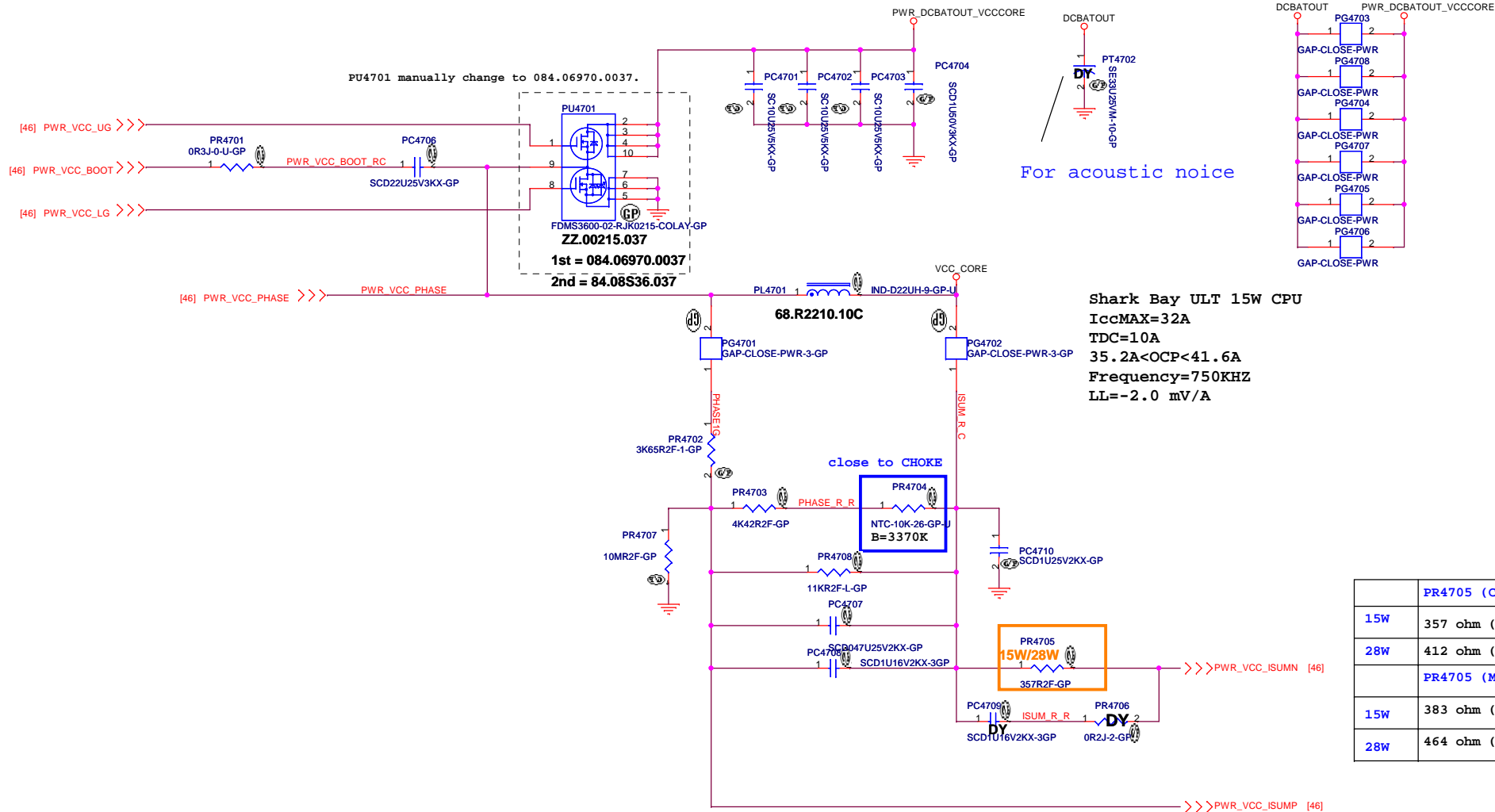


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Title	ISL95813_CPUCORE(1/2)
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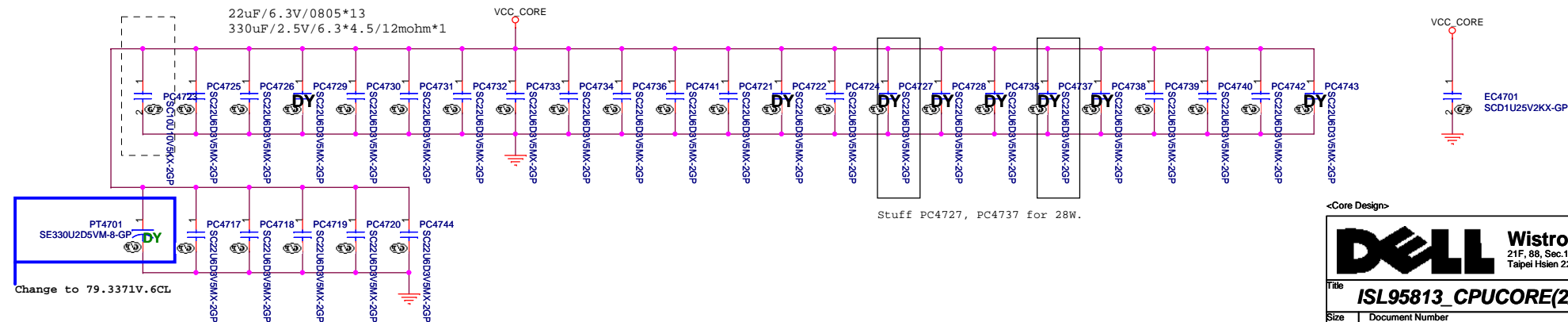
Size A3	Document Number Janus HSW 40/50/70	Rev A00
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Change PC4723 to 10U from 22U based on PI Simulation.

22uF/6.3V/0805*13
330uF/2.5V/6.3*4.5/12mohm*1



<Core Design>

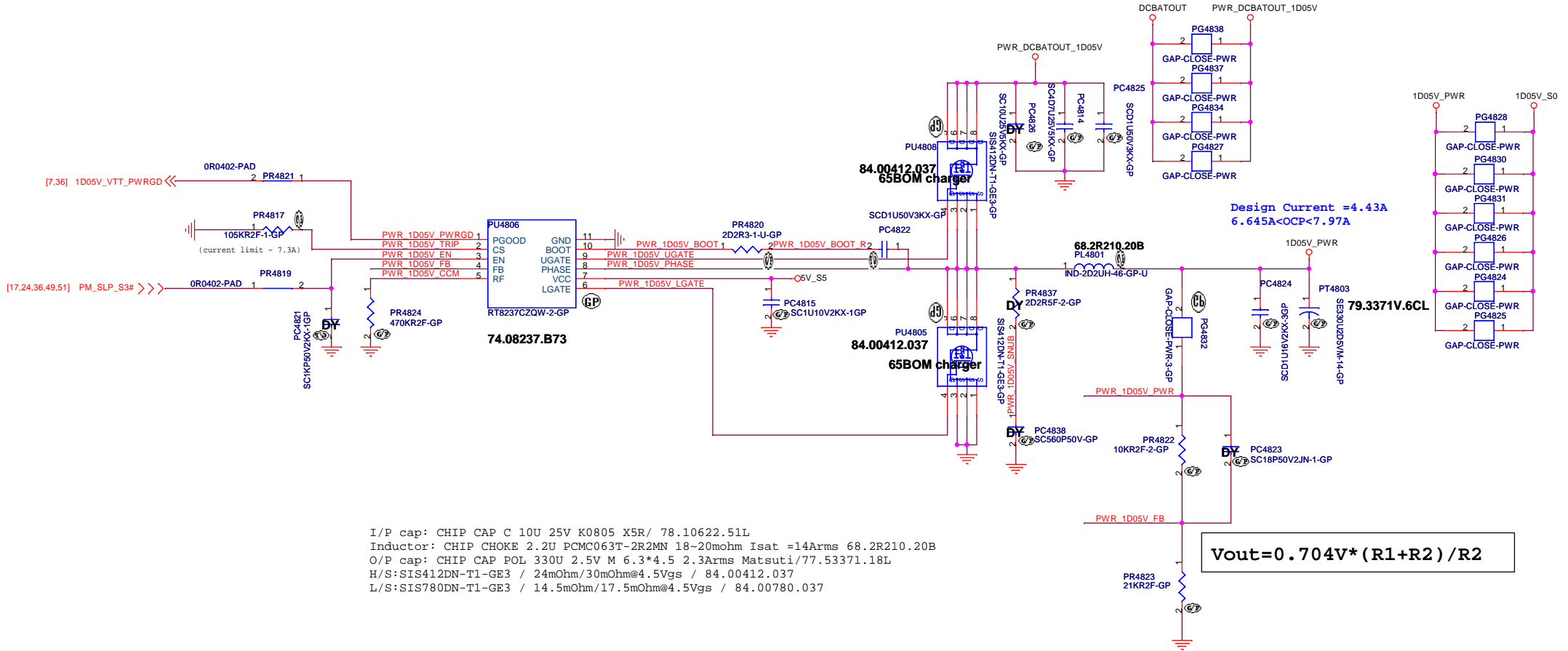
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95813 CPUCORE(2/2)**

Size: A3 Document Number: **Janus HSW 40/50/70** Rev: **A00**

Date: Friday, February 07, 2014 Sheet: 47 of 104

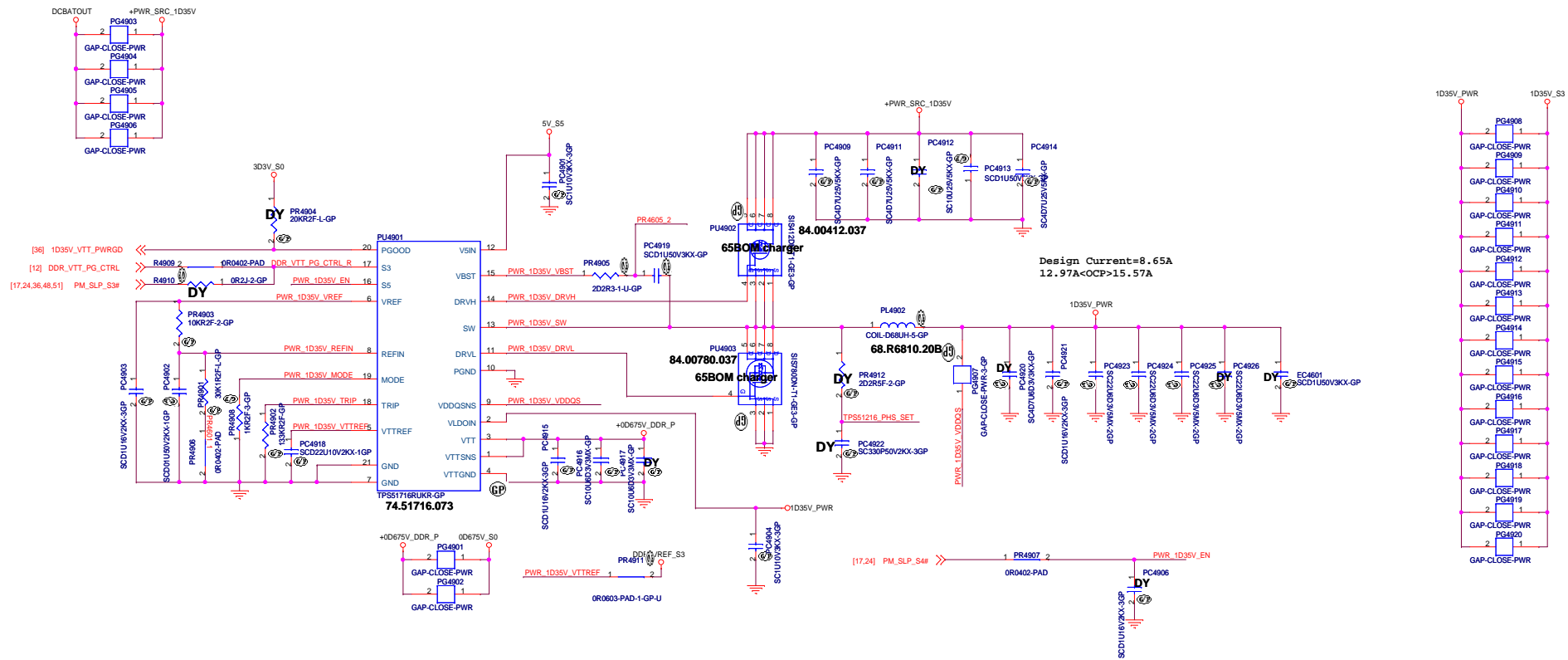
SSID = PWR.Plane.Regulator_1p05v



<Core Design>

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Title RT8237_1D05V			
Size A3	Document Number Janus HSW 40/50/70		Rev A00
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SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off


I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP IND 0.1uH M PCM0637P-R104M 1.5~1.7mohm Isat =60Arms 68.R1010.10T
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 MOS: FET MOS FDMS3664S NC POWER56 / 84.03664.037 / Q1: 8.5-11mohm @Vgs=4.5V Q2: 2.6-3.2mohm @Vgs=4.5V

<Core Design>

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File TPS51716_1D35V_S3			
Size C	Document Number Janus HSW 40/50/70		Rev A00
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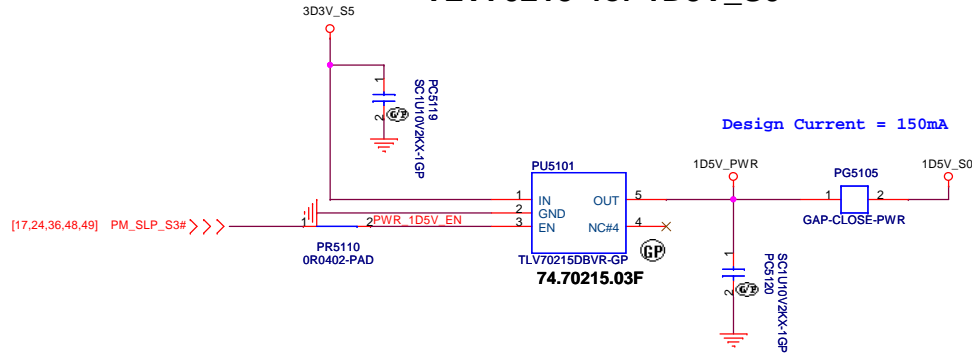
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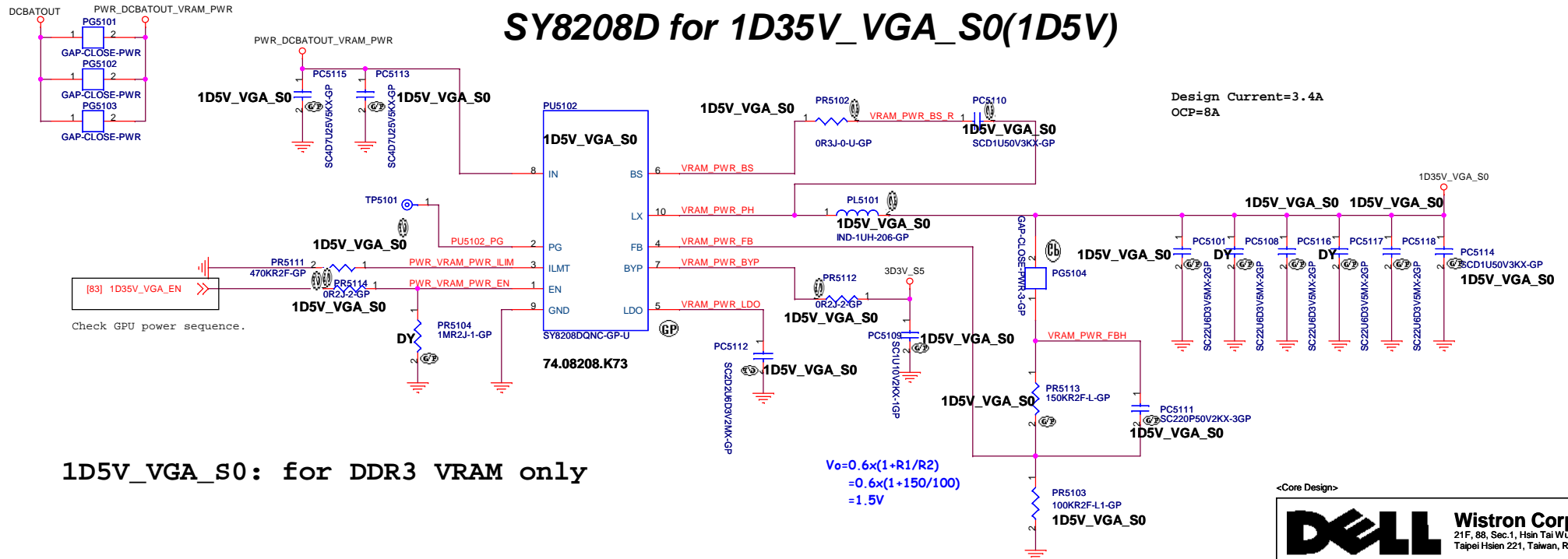
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Title Reserved			
Size A3	Document Number Janus HSW 40/50/70		Rev A00
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SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



1D5V_VGA_S0: for DDR3 VRAM only

$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 150/100) = 1.5V$$

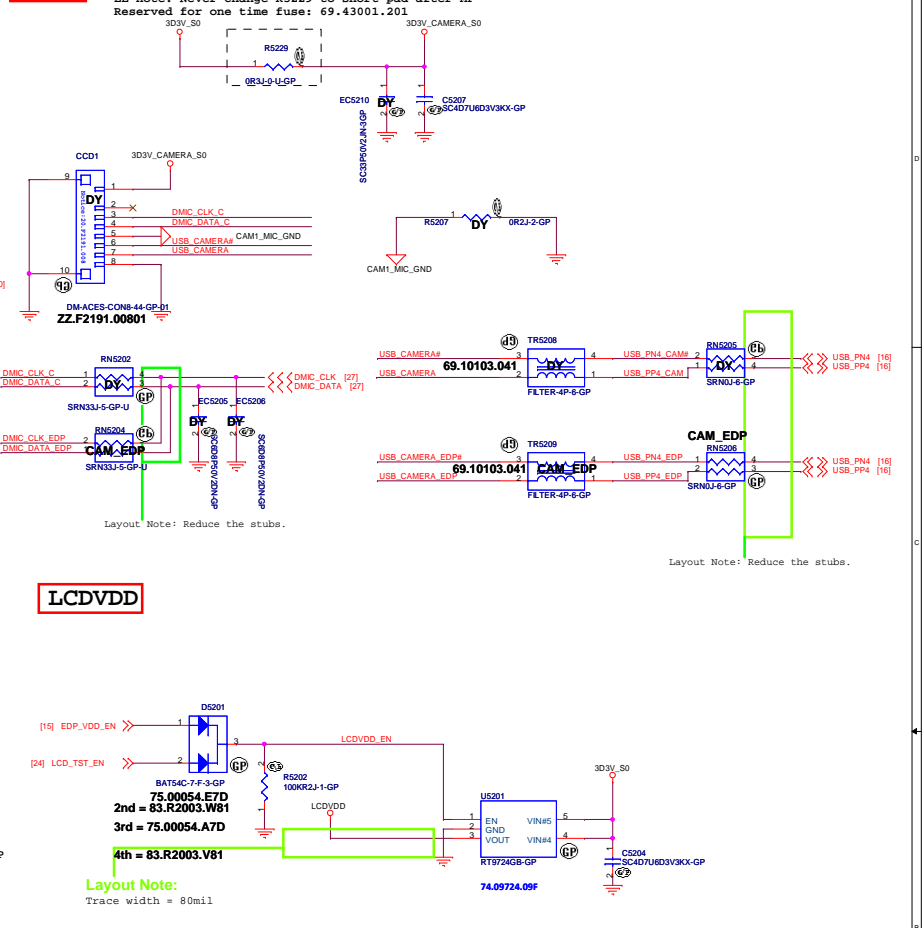
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Title: TLV70215_1D5V / SY8208D_1D5V(VGA)

Size: A3 Document Number: Janus HSW 40/50/70 Rev: A00

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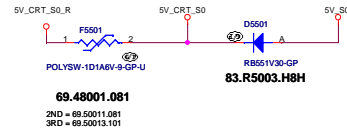
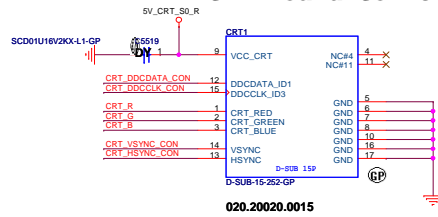
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Size	Document Number			Rev
A3	Janus HSW 40/50/70			A00
Date: Friday, February 07, 2014		Sheet 53 of 104		

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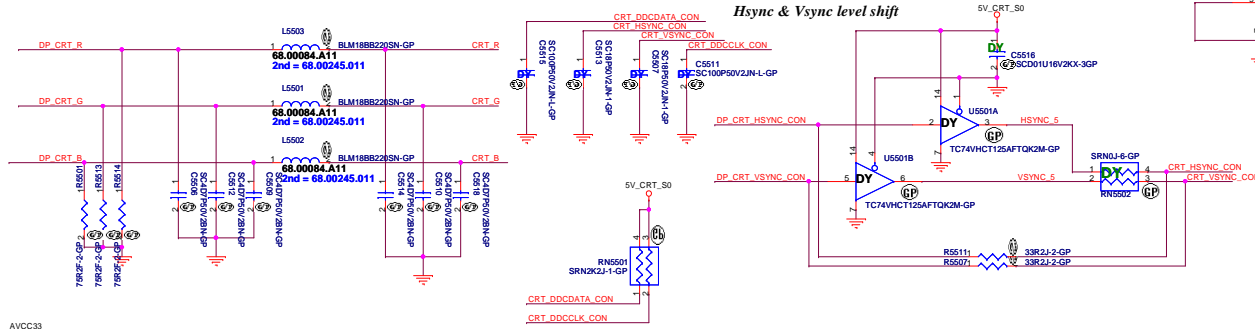
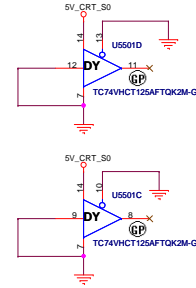
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Size A3	Document Number Janus HSW 40/50/70		Rev X02
Date: Friday, February 07, 2014	Sheet	54	of 104

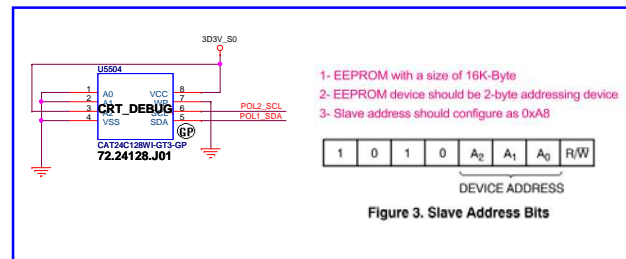
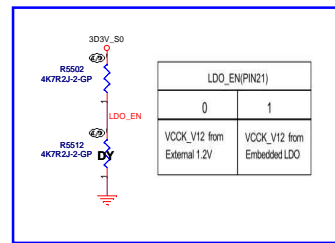
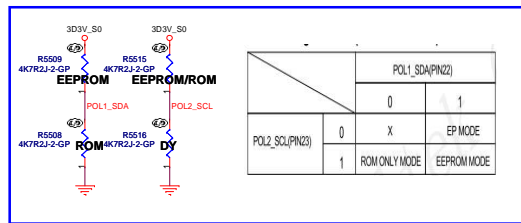
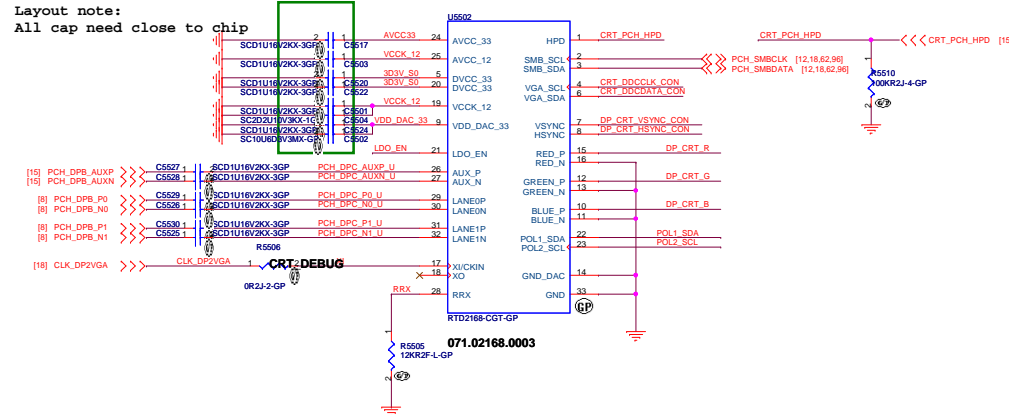
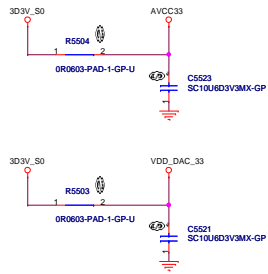
CRT Board Connector



**CRT RGB
CRT H/VSYNC
CRT SMBUS**



Layout note:
All cap need close to chip



- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

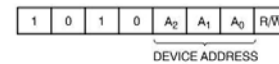
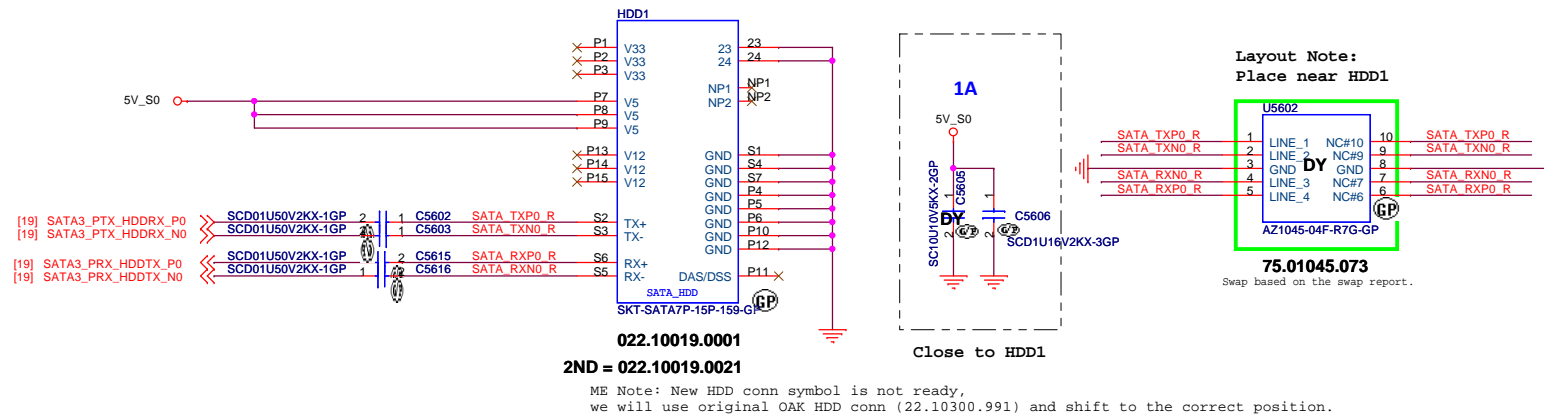


Figure 3. Slave Address Bits

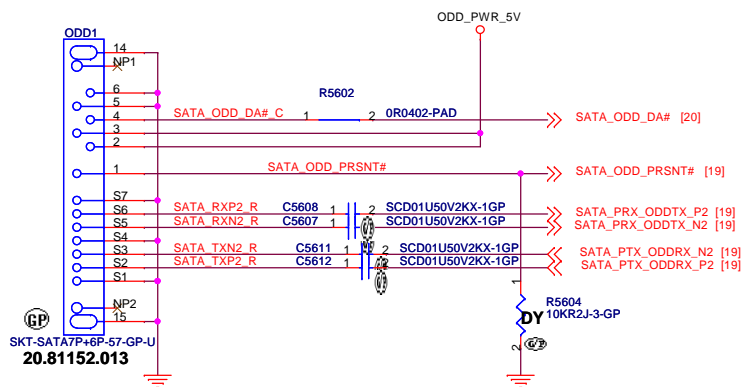
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SSID = SATA

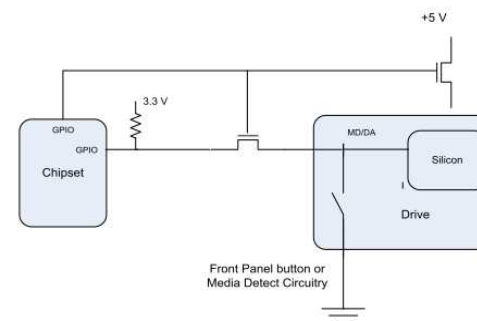
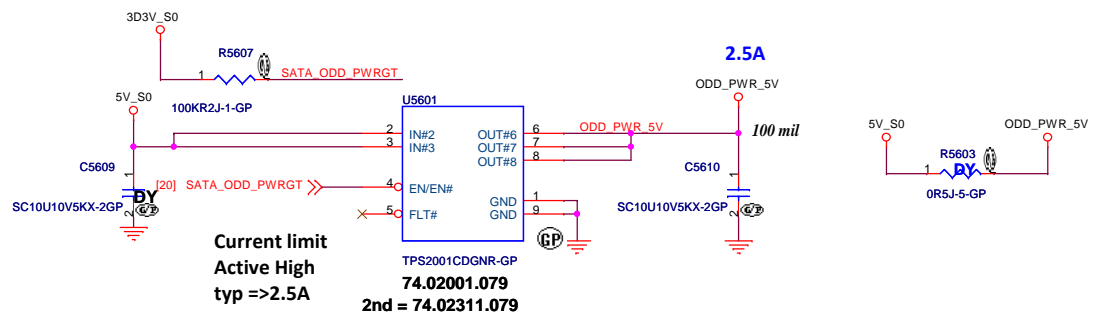
SATA HDD Connector



ODD Connector



SATA Zero Power ODD




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File			
HDD/ODD			
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SSID = ESATA

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<Core Design>



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Title

ESATA

Size

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Title

Mini Card (WLAN)

Size
A4

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<Core Design>



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Title

Reserved

Size
A4

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<Core Design>



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Title

(Reserved)

Size
A4

Document Number

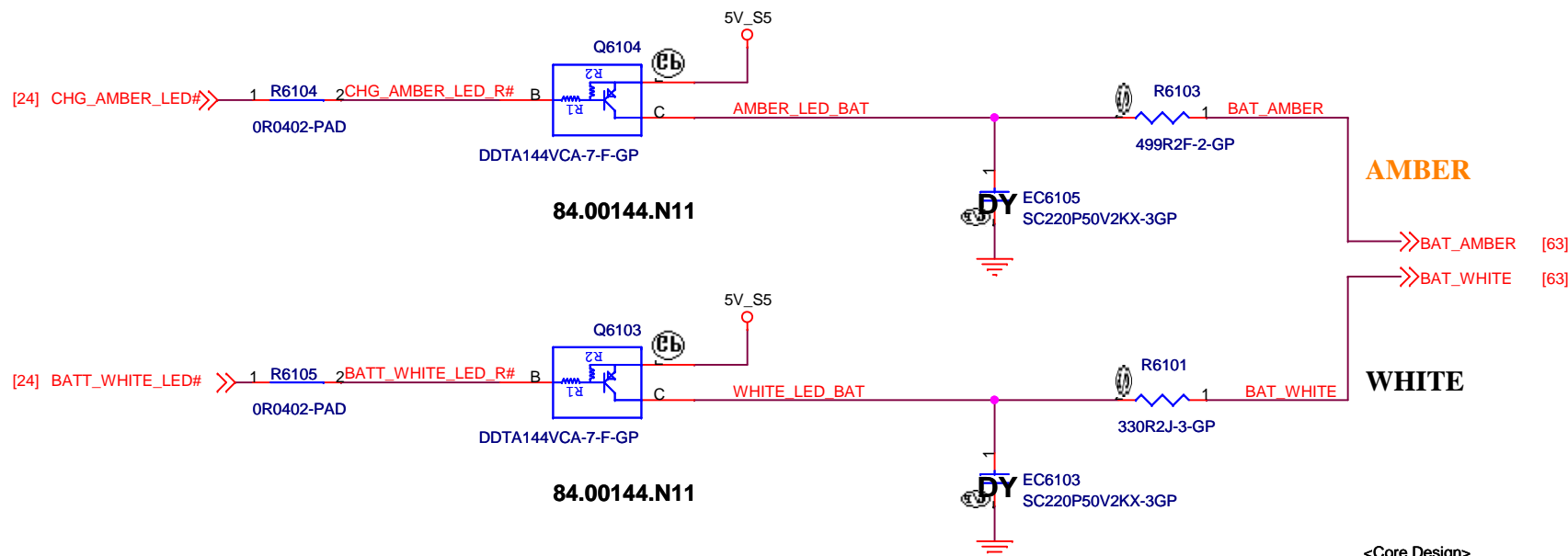
Janus HSW 40/50/70

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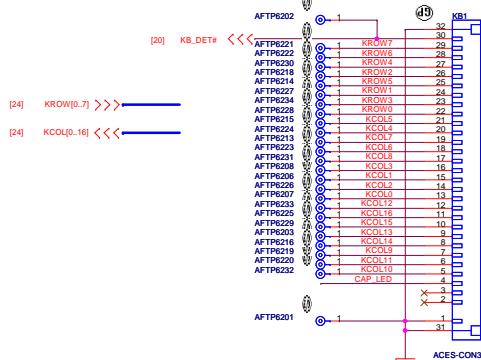
Battery LED1 (AMBER_LED)
Low activated from KBC GPIO



Battery LED2 (WHITE_LED)
Low activated from KBC GPIO

SSID = KBC

Internal Keyboard Connector (DVC40)



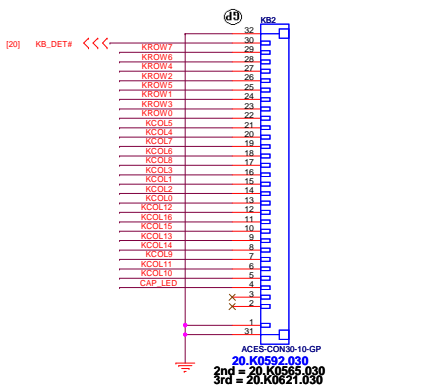
CAP LED Control

LOW acted from KBC GPIO



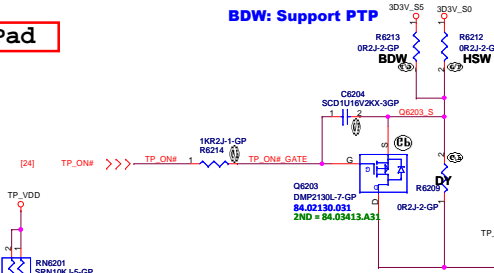
84.00144.N11

Internal Keyboard Connector (DVC50/DVC70)

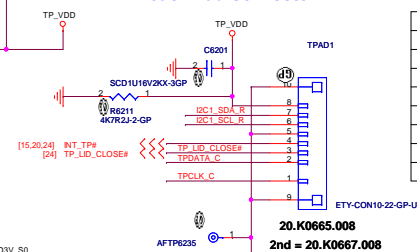


SSID = Touch.Pad

BDW: Support PTP



Touch Pad Connector



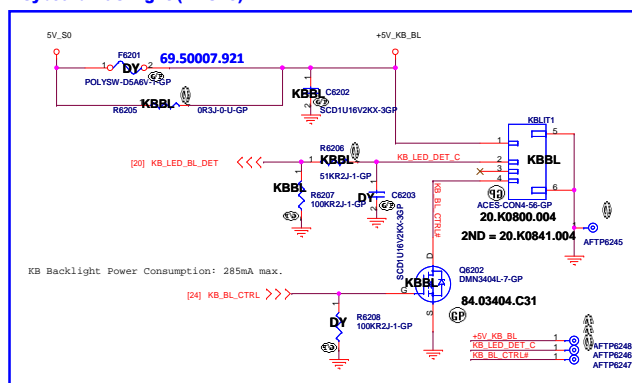
Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(P2)
8	CLK(P2)

PS2
I2C

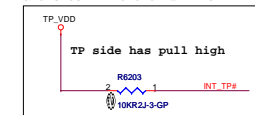
SMBUS

Need to check with SW.

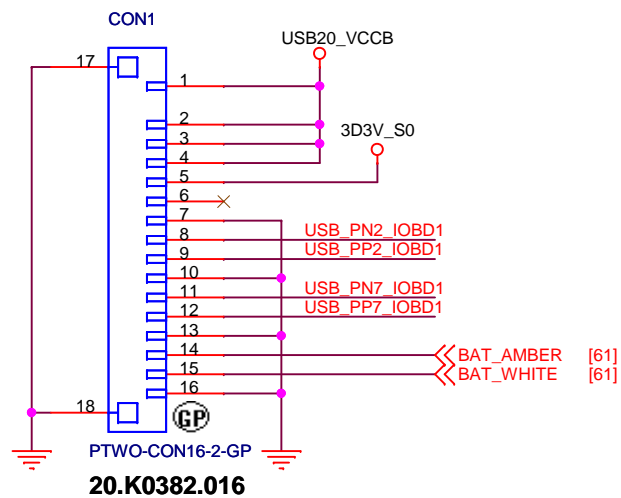
Keyboard Backlight (DVC70)



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

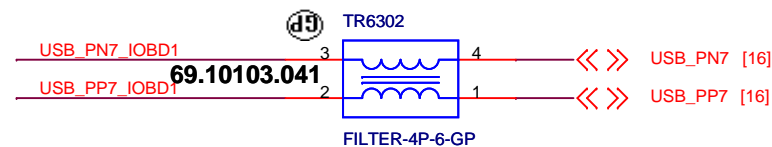
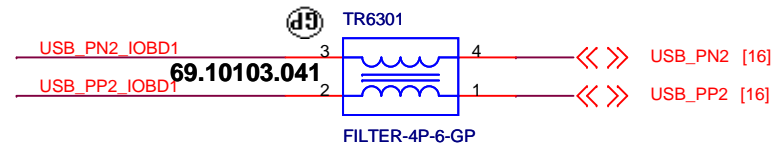
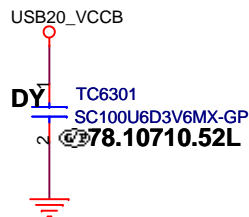


<Core Design>



USB2.0 Port3 Card Reader LED

The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



<Core Design>



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Title

IO Board Connector

Size
A4

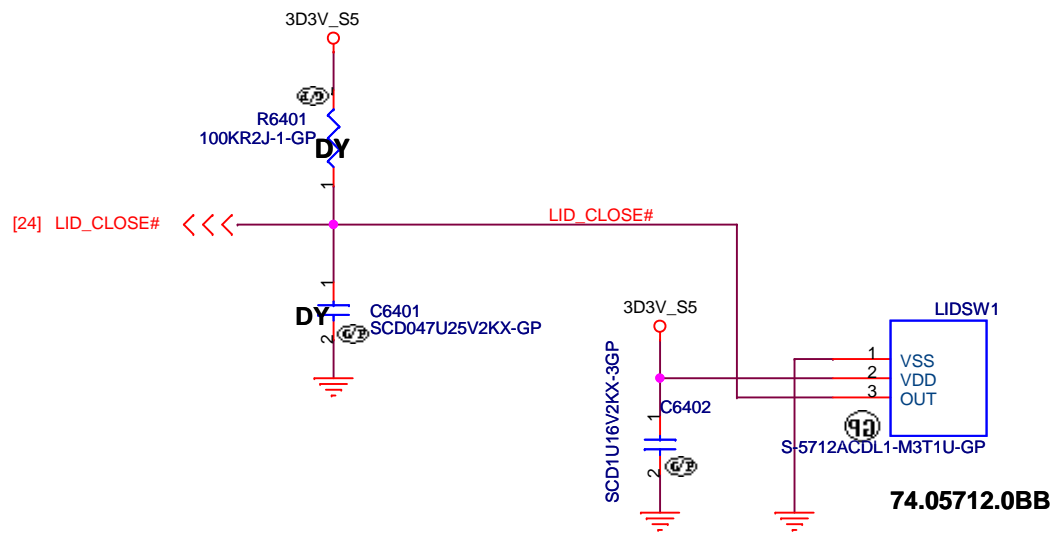
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SSID = User.Interface



<Core Design>



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Title

Hall Sensor

Size
A4

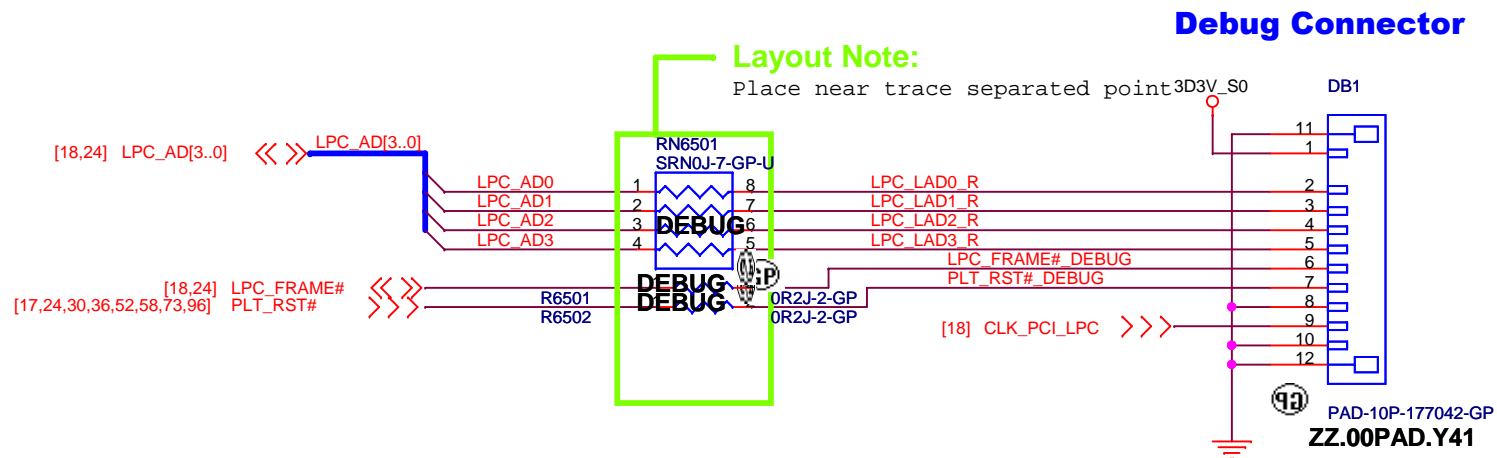
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20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>



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Title

Dubug connector

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Title			Reserved		
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<Core Design>



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<Core Design>



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Title

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<Core Design>



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Title

USB3.0 PORT

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<Core Design>

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Title			
Reserved			
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<Core Design>

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Title			
Reserved			
Size	Document Number		Rev
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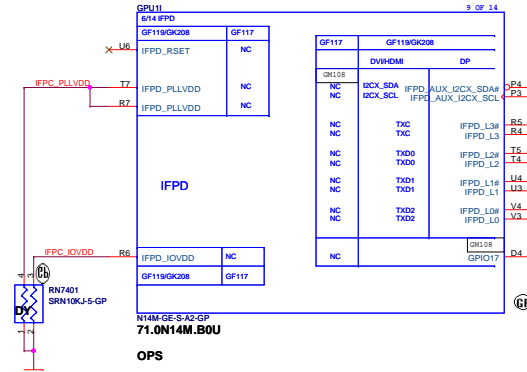
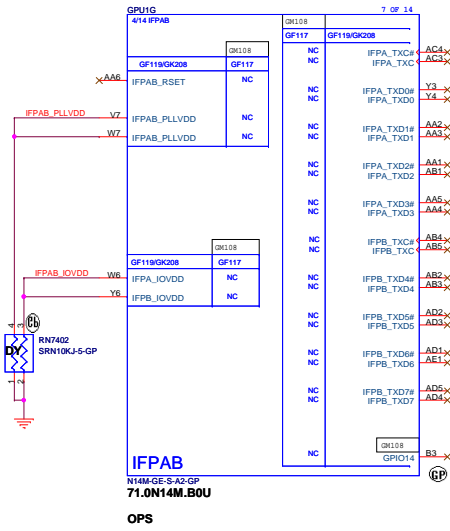
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Janus HSW 40/50/70		Rev A00
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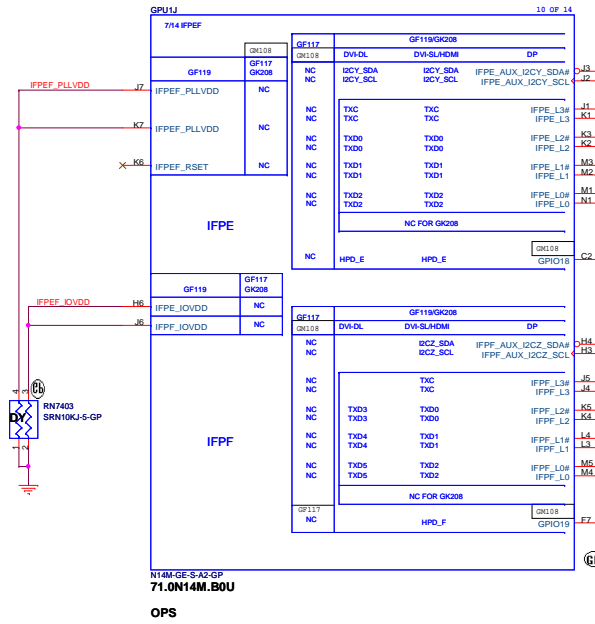
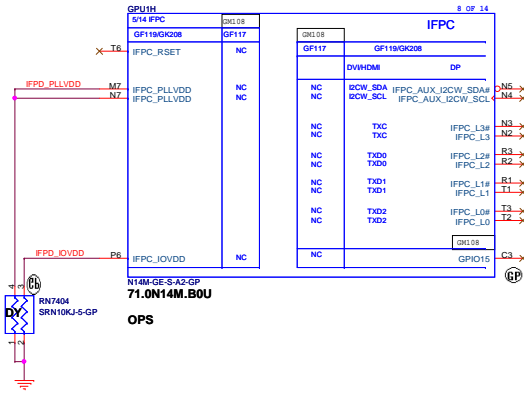


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Title	
GPU PCIE/STRAPPING(1/5)	
Size A2	Document Number Janus HSW 40/50/70
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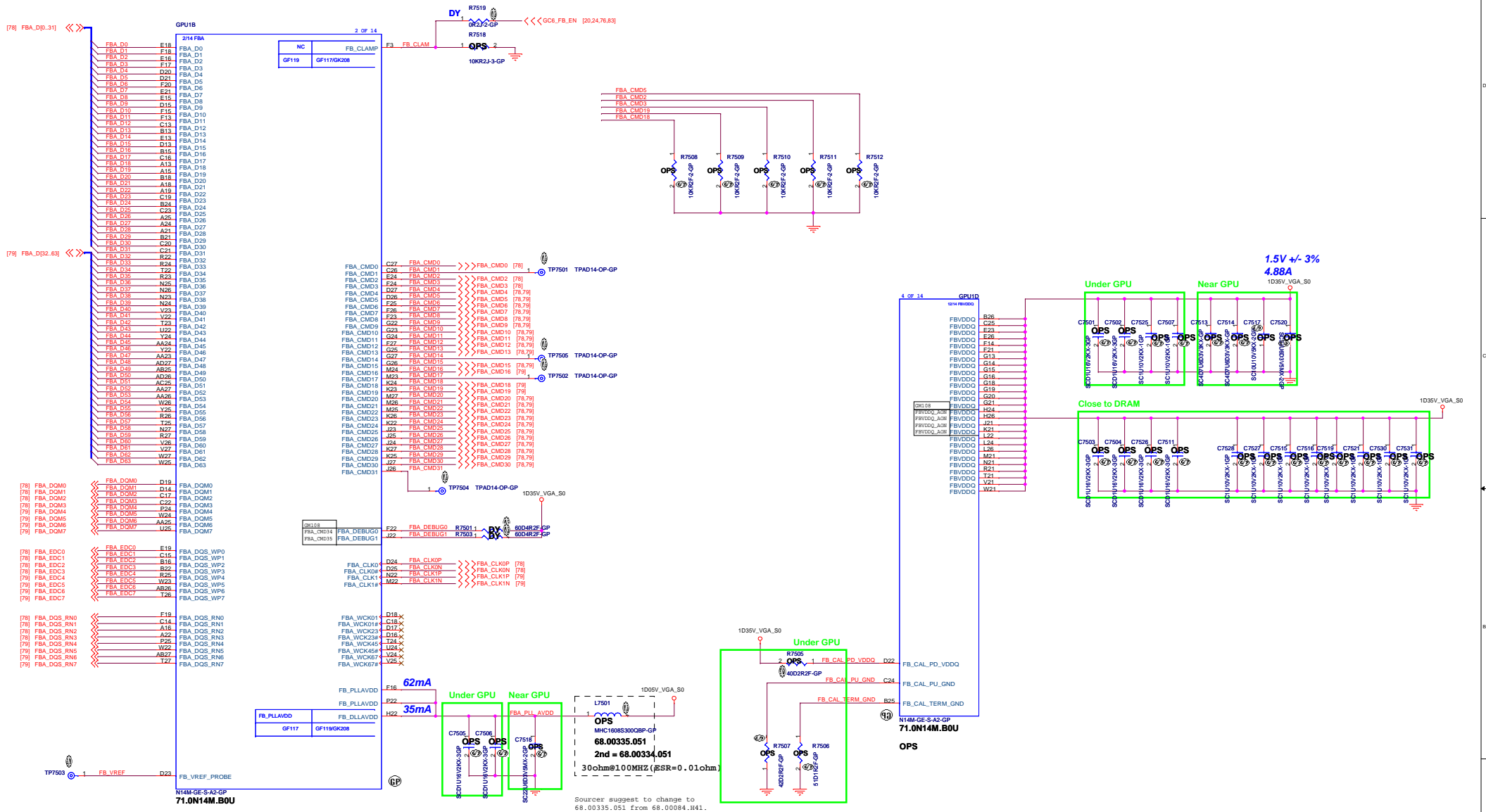
LVDS Interface



HDMI Interface

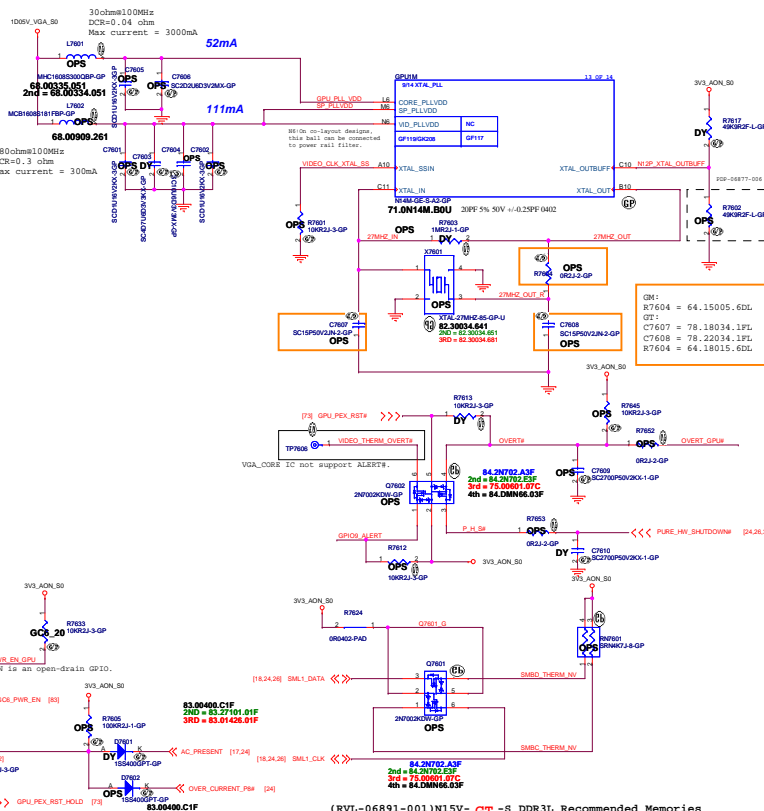
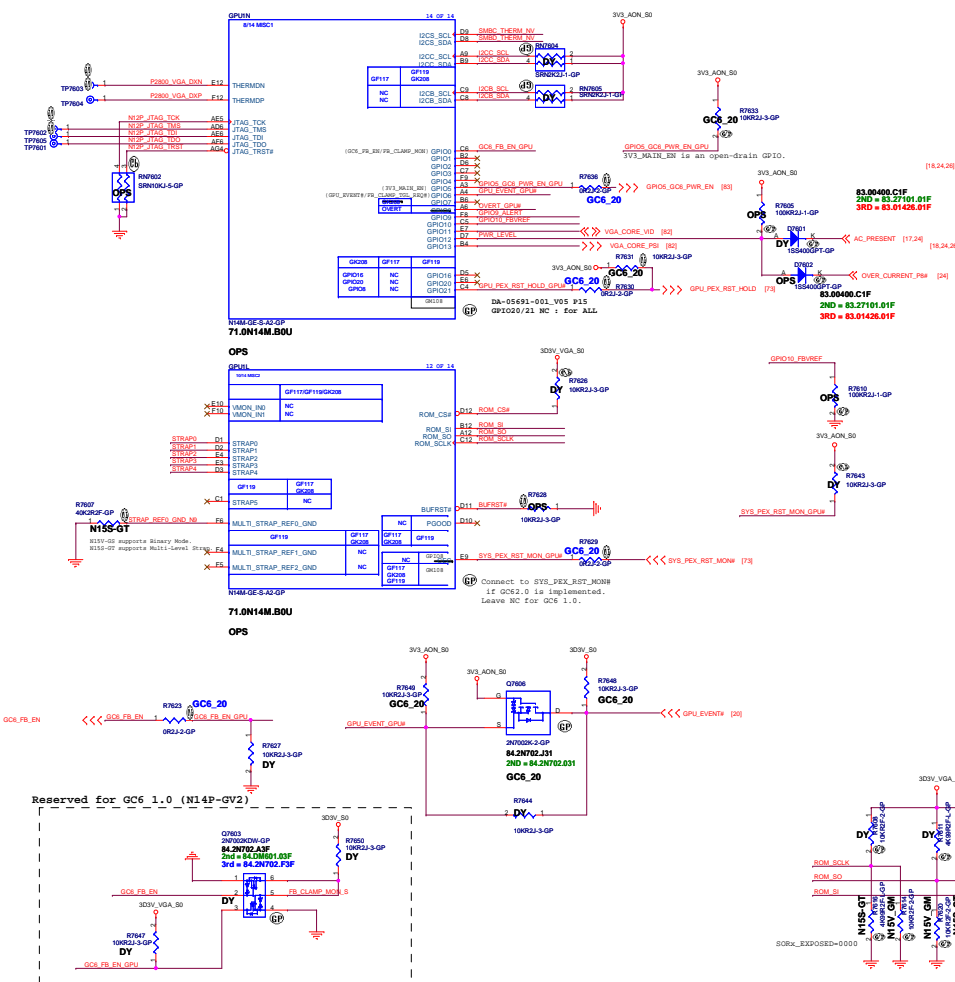


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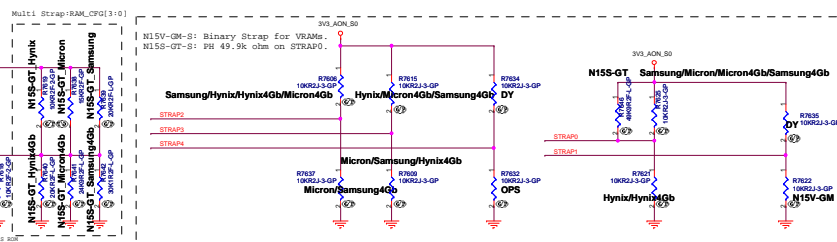
GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2E-64 and GB4B-128	PLLVD	0.1 μ F X7R	0402	1	Under GPU
		22 μ F X5R	0805	1	Near GPU
		Bead Type			
		30 Ω (ESR=0.05)	0402	1	Near GPU

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
G82B-64	SP_PLLVDD + VID_PLLVDD	0.1 μ F X7R	0402	1 per ball	Under GPU
G84B-128		4.7 μ F X5R	0603	1	Near GPU
G83-256		22 μ F X5R	0805	1	Near GPU
Bead Type					
		180 Ω (ESR=0.2)	0603	1	Near GPU



		Strap	
128Mx16 DDR3L	Hynix	0x9	H5TC2G63FFR-11C
	Micron	0xA	MT41K128M16JT-107G:R
	Samsung	0xB	K4W2G1G646E-BY11
256Mx16 DDR3L	Hynix	0x3	H5TC4G63AFR-11C
	Micron	0x4	MT41K256M16A-107G:R
	Samsung	0x5	K4W4G1G646D-BC1A

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VEHIDOR	10kΩ	<ul style="list-style-type: none"> • Pull-up to 3V3 if VBIOS ROM exists • Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

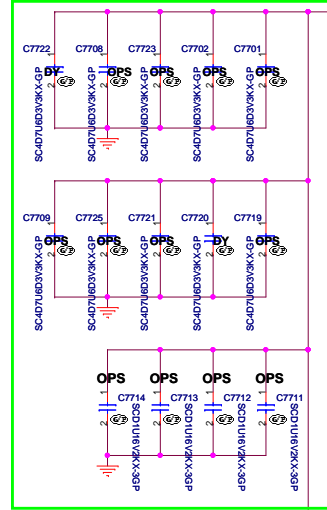
		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	0xC	H5TC2G63FFR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	H1155-GV H1155-GM/-GT	PCI_DEVID[4] S0R3_EXPOSED	SUB_VENDOR S0R2_EXPOSED	PCI_DEVID[5] S0R1_EXPOSED	PEX_PLL_EH_TERM S0R0_EXPOSED
ROM_SI	All GB2-64 H1155 and GB2B-64 H115	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	H1155-GV H1155-GM/-GT	FB[1]	FB[0]	SUB_ALT_ADDR	VGA_DEVICE
STRAP0	H1155-GV H1155-GM/-GT	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	H1155-GV H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff S0M pull-up) 3G00_PADCFG[3] 3G00_PADCFG[2] 3G00_PADCFG[1] 3G00_PADCFG[0]			
STRAP2	H1155-GV H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default) PCI_DEVID[3] PCI_DEVID[2] PCI_DEVID[1] PCI_DEVID[0]			
STRAP3	H1155-GV H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default) S0R3_EXPOSED S0R2_EXPOSED S0R1_EXPOSED S0R0_EXPOSED			
STRAP4	H1155-GV H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default) RESERVED PCIE_SPEED_CHA HGE_GE13 PCIE_MAX_SPEED DP_PLL_VDD033V			

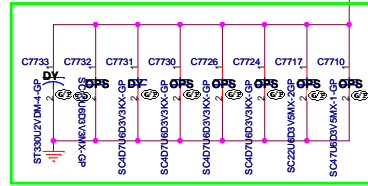
	SDR-0012	SDR-0013
Chip	N15V-GM	N155-GT
Device ID	N15V-GM	N155-GT
Device ID	0x1140	0x1341
Memory Interface	sDDR3	sDDR3
Package	S95 ball BGA 23x23mm	S95 ball BGA 23 x 23 mm - 908 ball BGA 29 x 29 mm



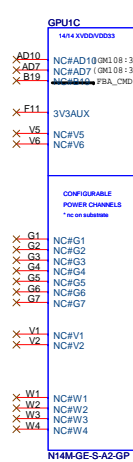
Under GPU



Near GPU



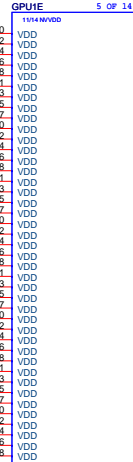
G10, G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.

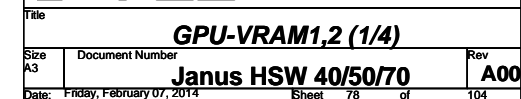


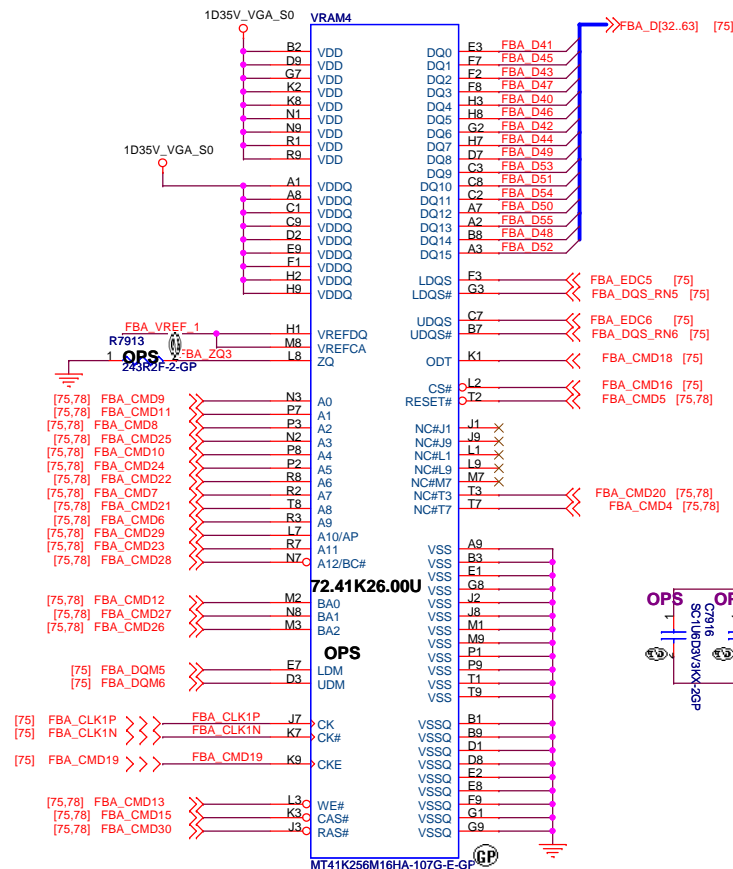
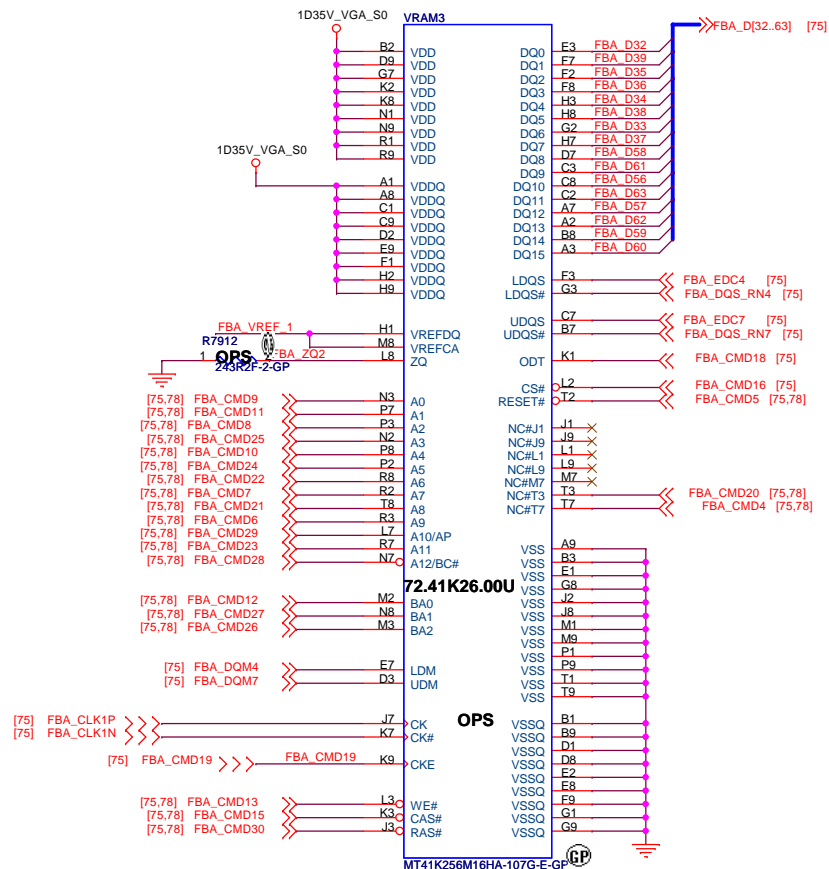
71.0N14M.B0U

OPS

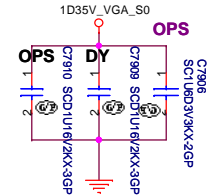
VGA_CORE



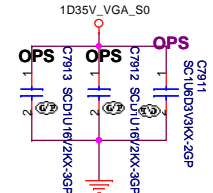




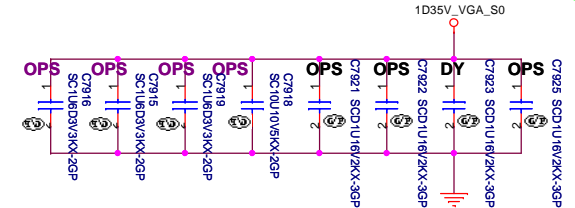
Place close VRAM3 VDD ball



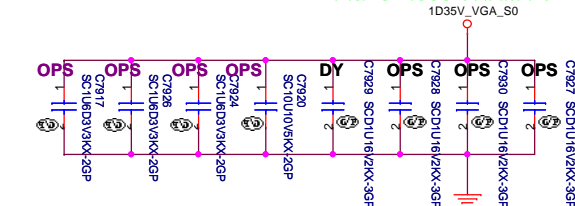
Place close VRAM4 VDD ball



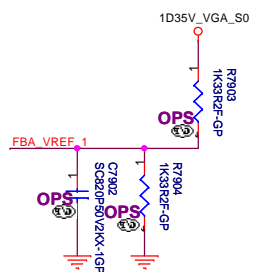
Place close VRAM3 VDDQ ball



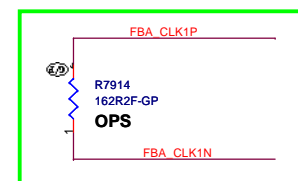
Place close VRAM4 VDDQ ball



Frame Buffer Patition A-Lower Half



FBCLK Termination place on VRAM side



Layout Note: Place in the end.

<Core Design>



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Title

GPU-VRAM3,4 (2/4)

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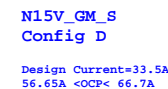
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Title		
GPU-VRAM5,6 (3/4)		
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<Core Design>		
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title GPU-VRAM7,8 (4/4)		
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Component value	N15V-QM-S Config D	N15-S-G7-S Config B
R1 (PR8222)	27K 64.27025.6DL	20K 64.20025.6DL
R2 (PR8206)	7.5K 64.75015.6DL	20K 64.20025.6DL
R3 (PR8208)	0 63.R0034.1DL	2K 64.20015.6DL
R4+R5 (R28209)	7.87K 64.78715.6DL	18K 64.18025.6DL
C (PC8223)	5.6nF 64.56223.28F	2.7nF 64.27224.28F

PWA-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.6	0.9
Vmax	V	1.2	1.2	1.5	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	25	25	12.5
Number of Voltage Levels N	level	9	10	20	20
PWMA Frequency F_{PWA}	MHz	-	1.125	0.675	0.675
PWMA Minimum Pulse Width T_{PWA}	ns	9.25	74	74	74
VD Transient Time T	ns	<100	<100	<100	<100
Component Value					
R1 (15)	Ω	20	20	20	27
R2 (15)	Ω	20	20	20	7.5
R3 (15)	Ω	1.5	2	3	0
R4 (15)	Ω	30	18	24	6.2
R5 (15)	Ω	1.5	0	3	1.74
nF	fF	1.5	2.7	1.8	5.6

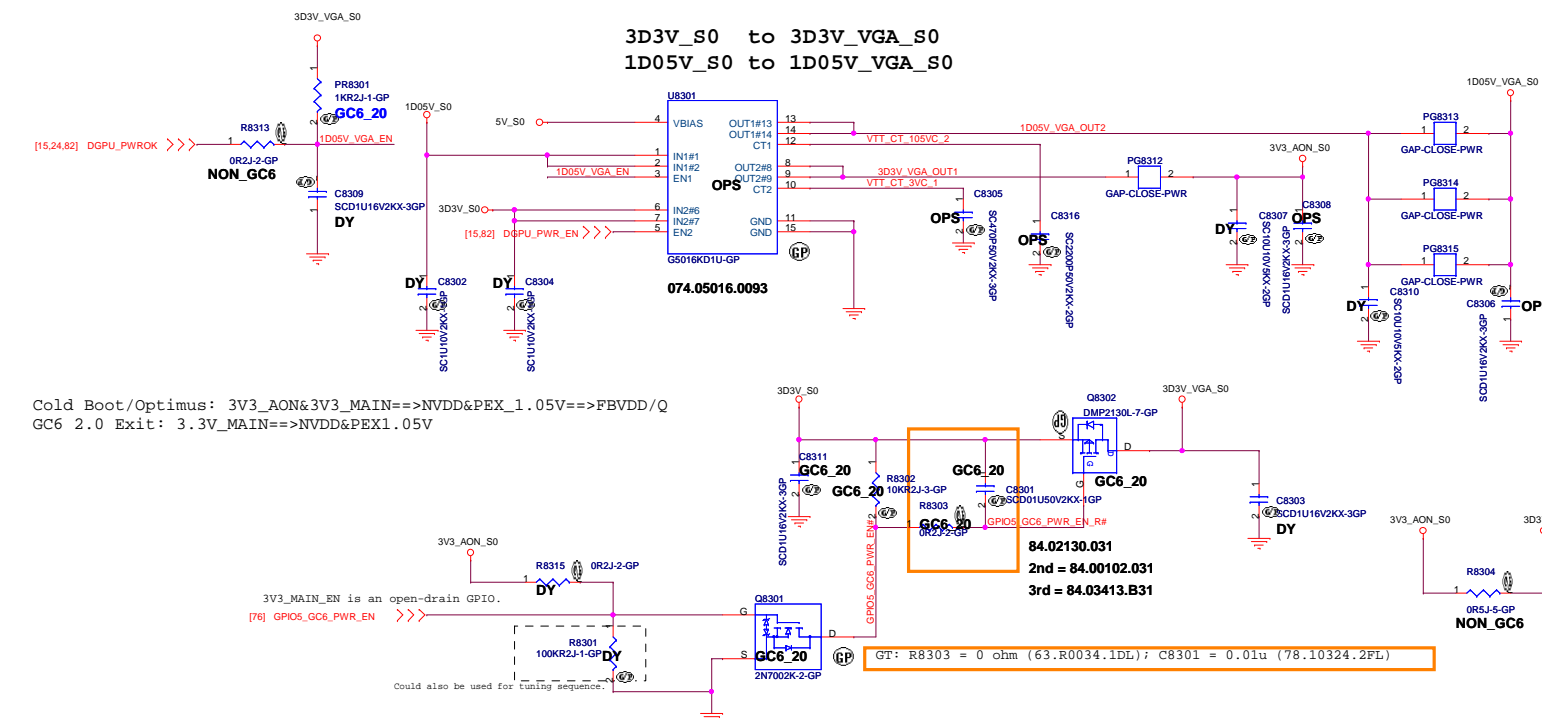
```
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 0.22UH PCCMC104T-R22/ 1mohm/ Isat =60A rms /68.2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6 3*4-R chem-coni/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mohm4.5Vgs/ 84.A14DP.037
L/S: SIRA06DP-T1-GE3 / 2.75mohm/3.5mohm4.5Vgs/ 84.SRA06.037
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◀Core Design:

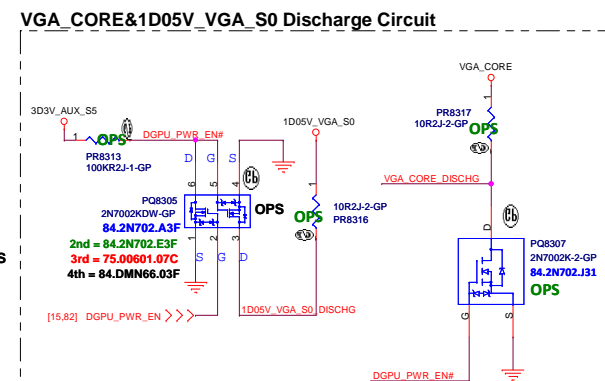


Title			
RT8812 VGACORE			
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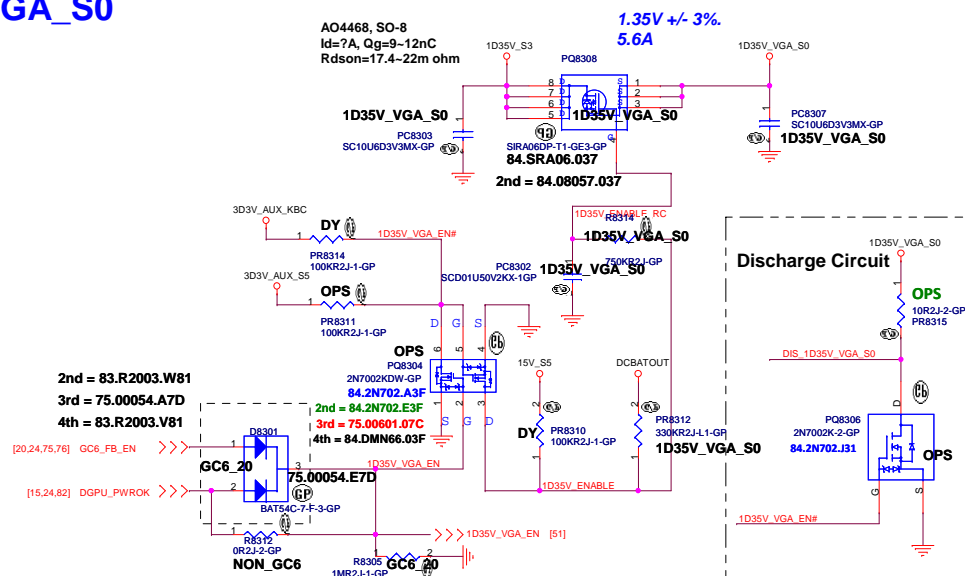
1D35V VGA S0 should ramp-up before 1D05V VGA S0



Cold Boot/Optimus: 3V3_AON&3V3_MAIN==>NVDD&PEX_1.05V==>FBVDD/Q
GC6 2.0 Exit: 3.3V MAIN==>NVDD&PEX1.05V



1D35V_VGA_S0



CTx (pF)	Rise Time (μs) 10% - 90%, COUT = 0.1μF @ VIN; VOUT=0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

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Title	DISCRETE VGA POWER
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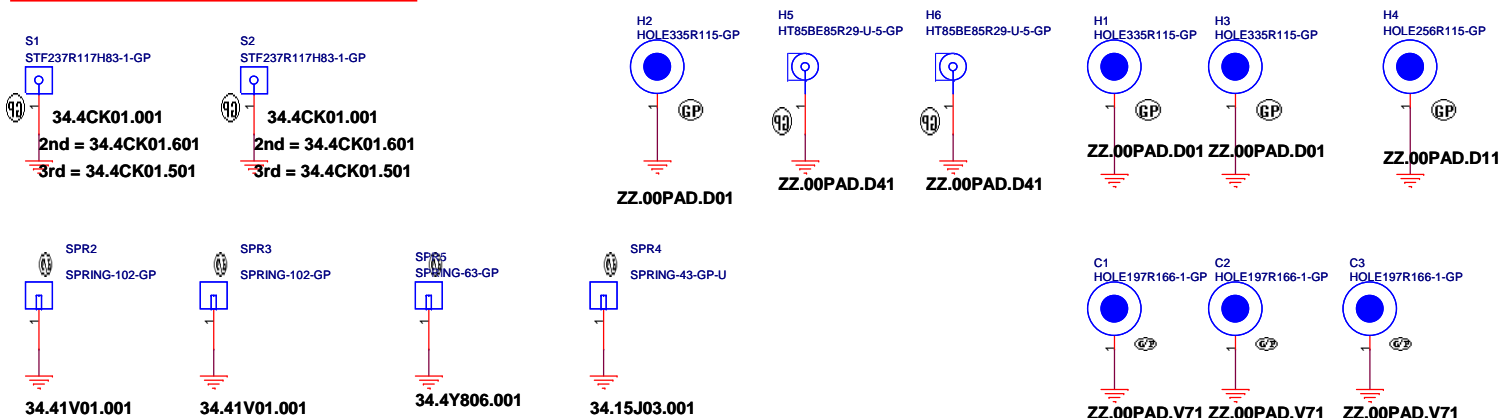
Rev

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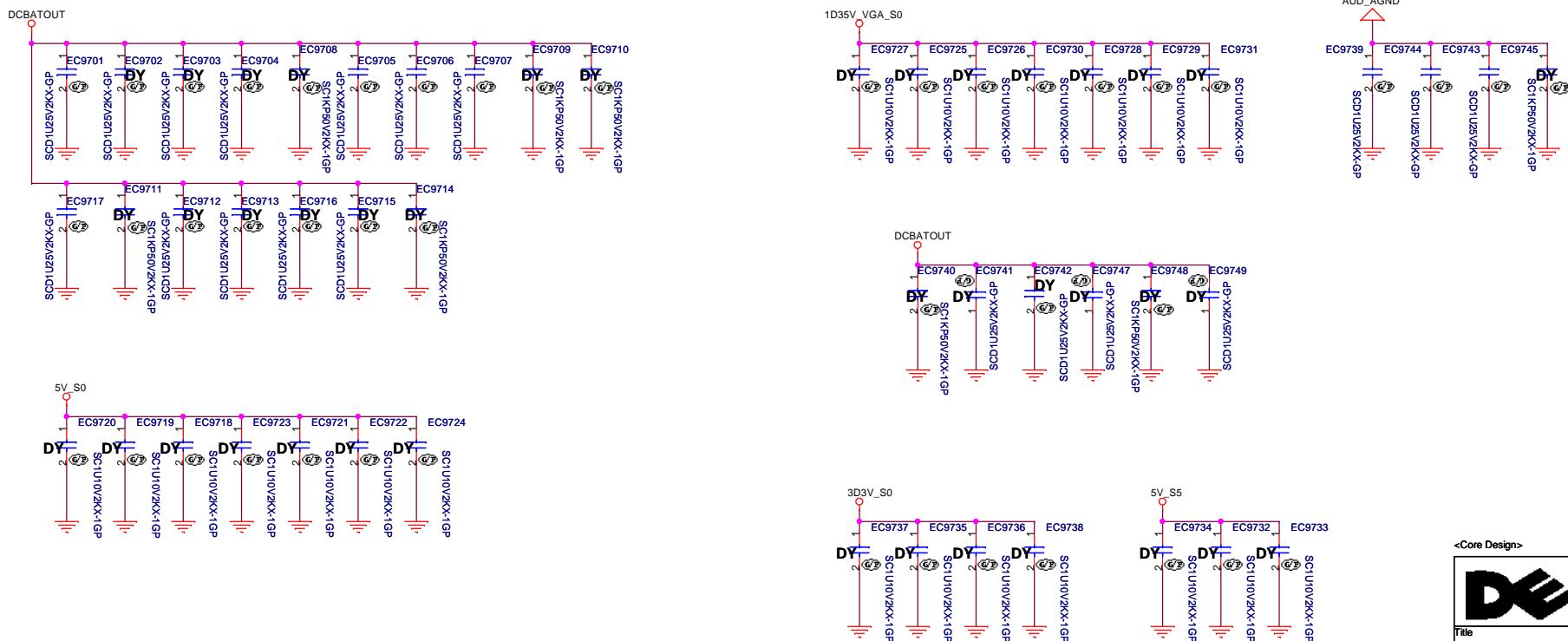
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SSID = Mechanical



SSID = EMI

Mind the voltage rating of the caps.



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Title
UNUSED PARTS/EMI Capacitors

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Title

Free Fall Sensor

Size
A3

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Title		
Express Card		
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Title LVDS Switch			
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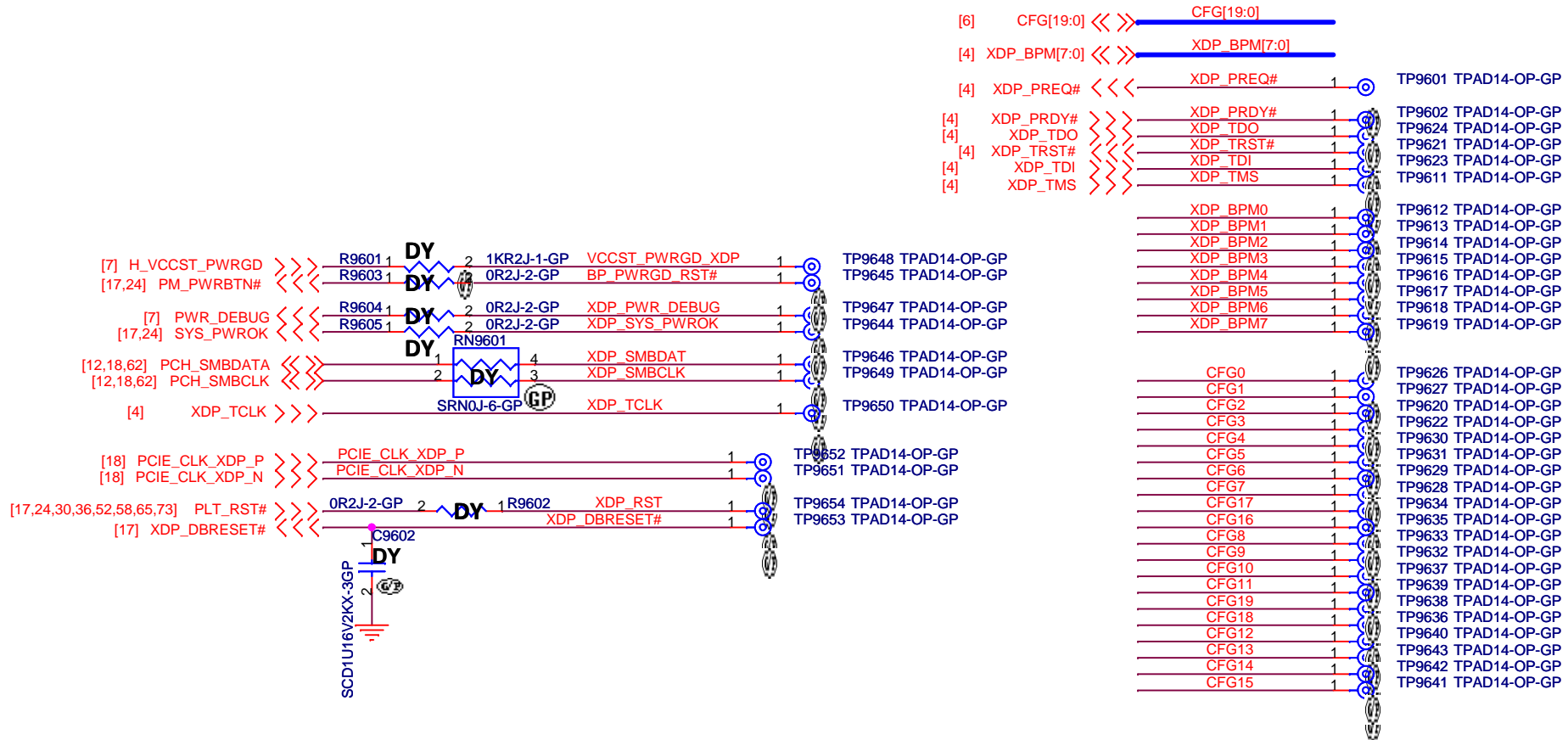
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Title			
CRT Switch			
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SSID = XDP

CPU XDP



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Title

CPU/PCH XDP

Size
A4

Document Number

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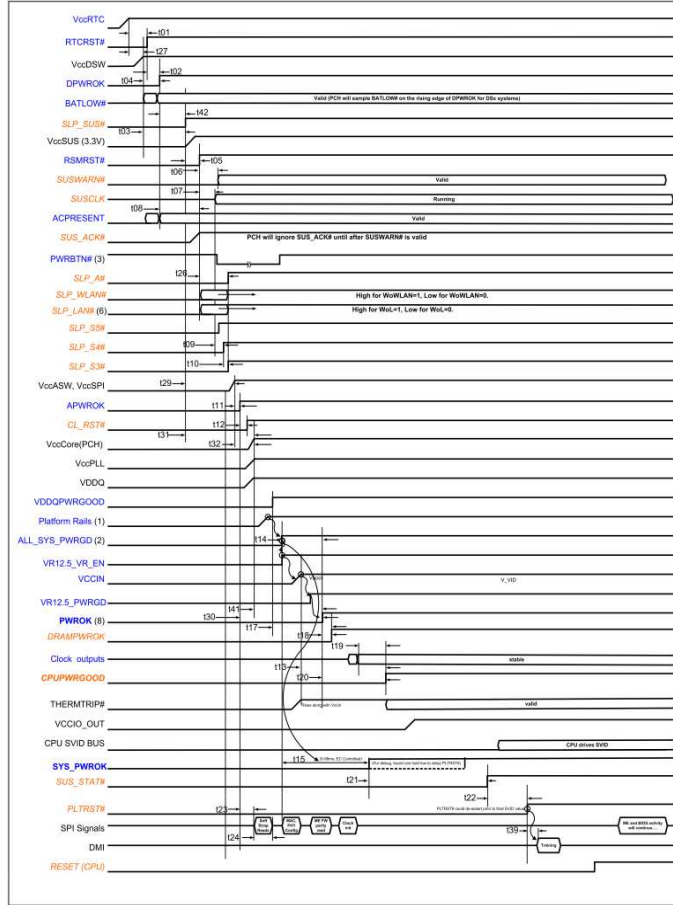
Rev

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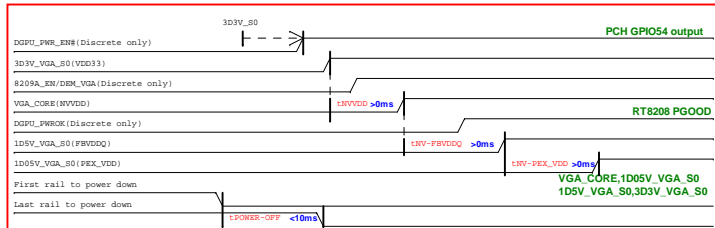
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Shark Bay Platform Power Sequence

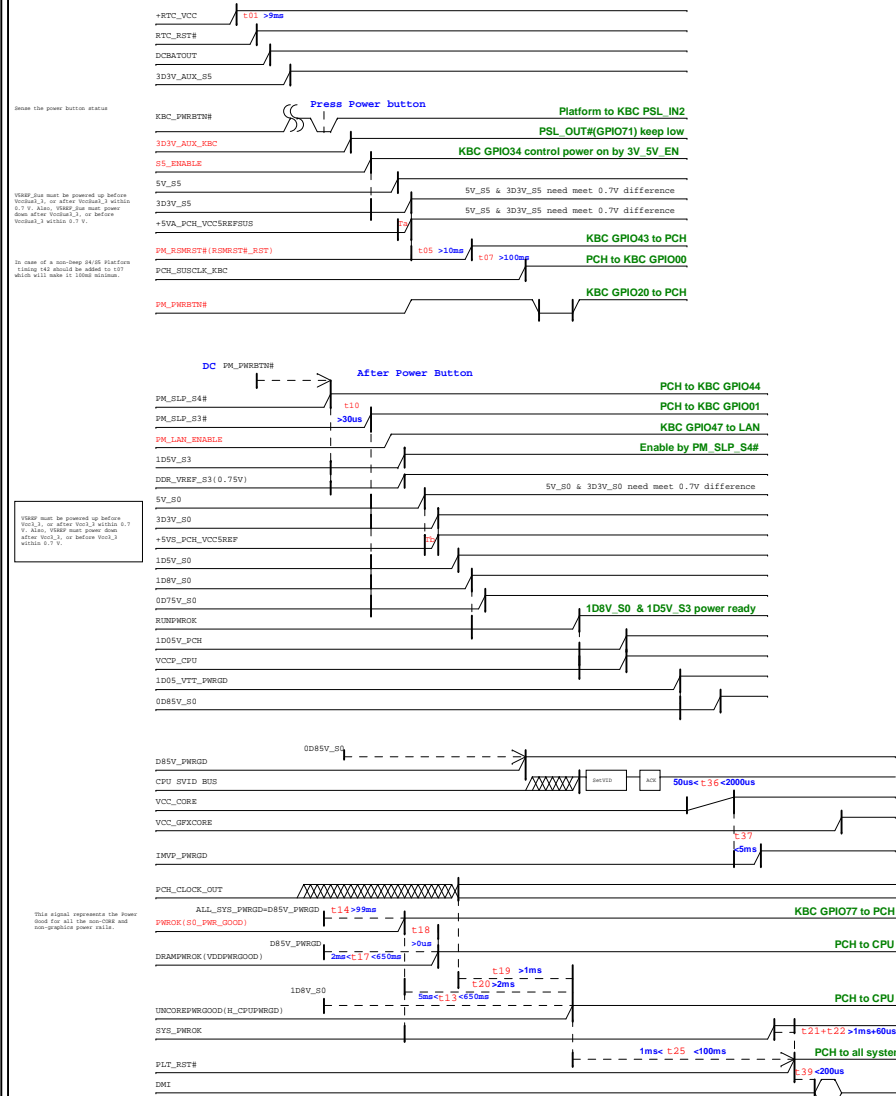


N14P-GT Power-Up/Down Sequence



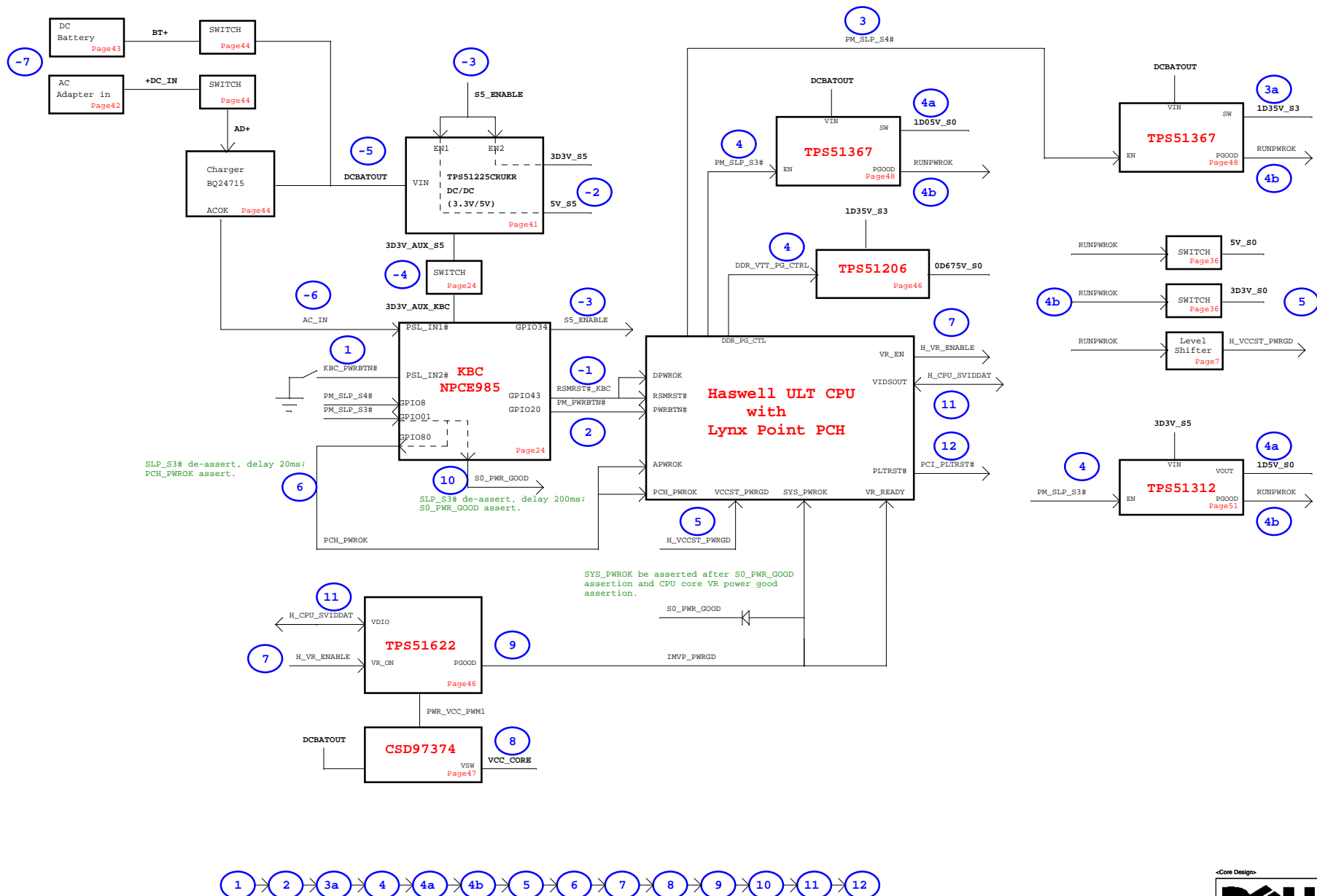
For power-down, reversing the ramp-up sequence is recommended.

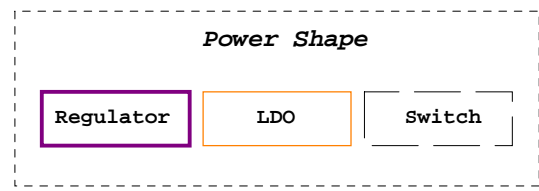
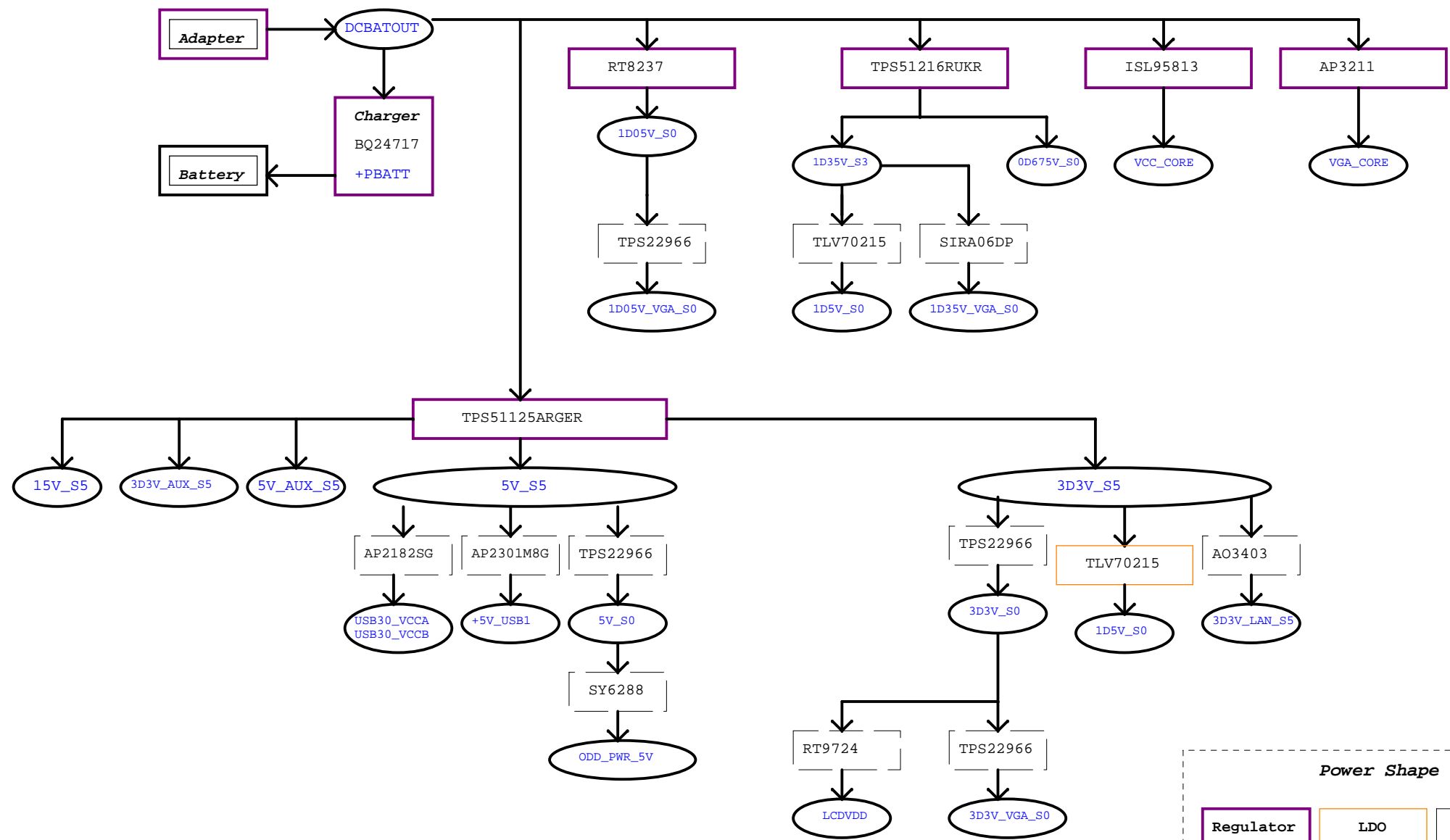
(DC mode)



This signal represents the power good for all the non-CPU and non-graphic power rails.

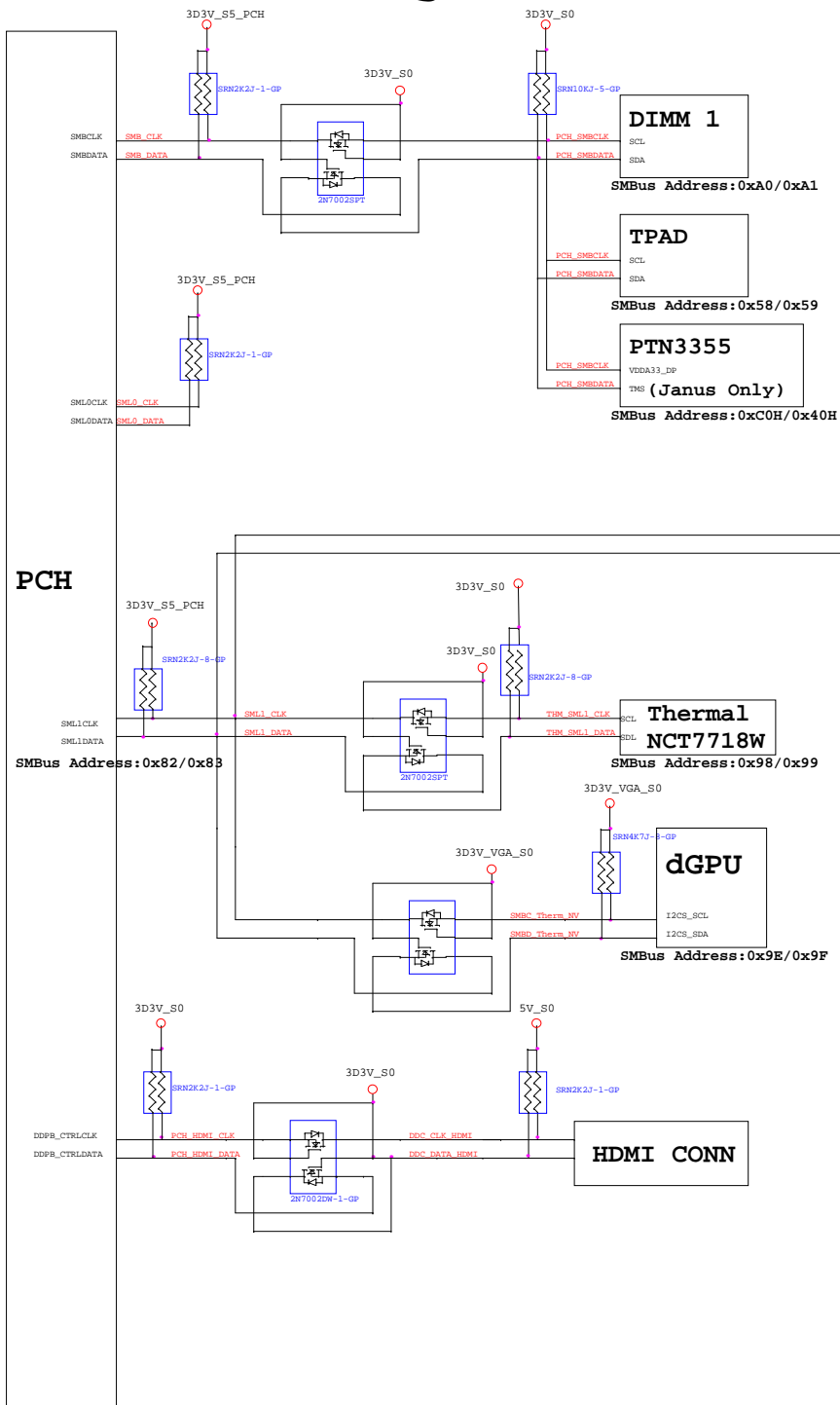
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



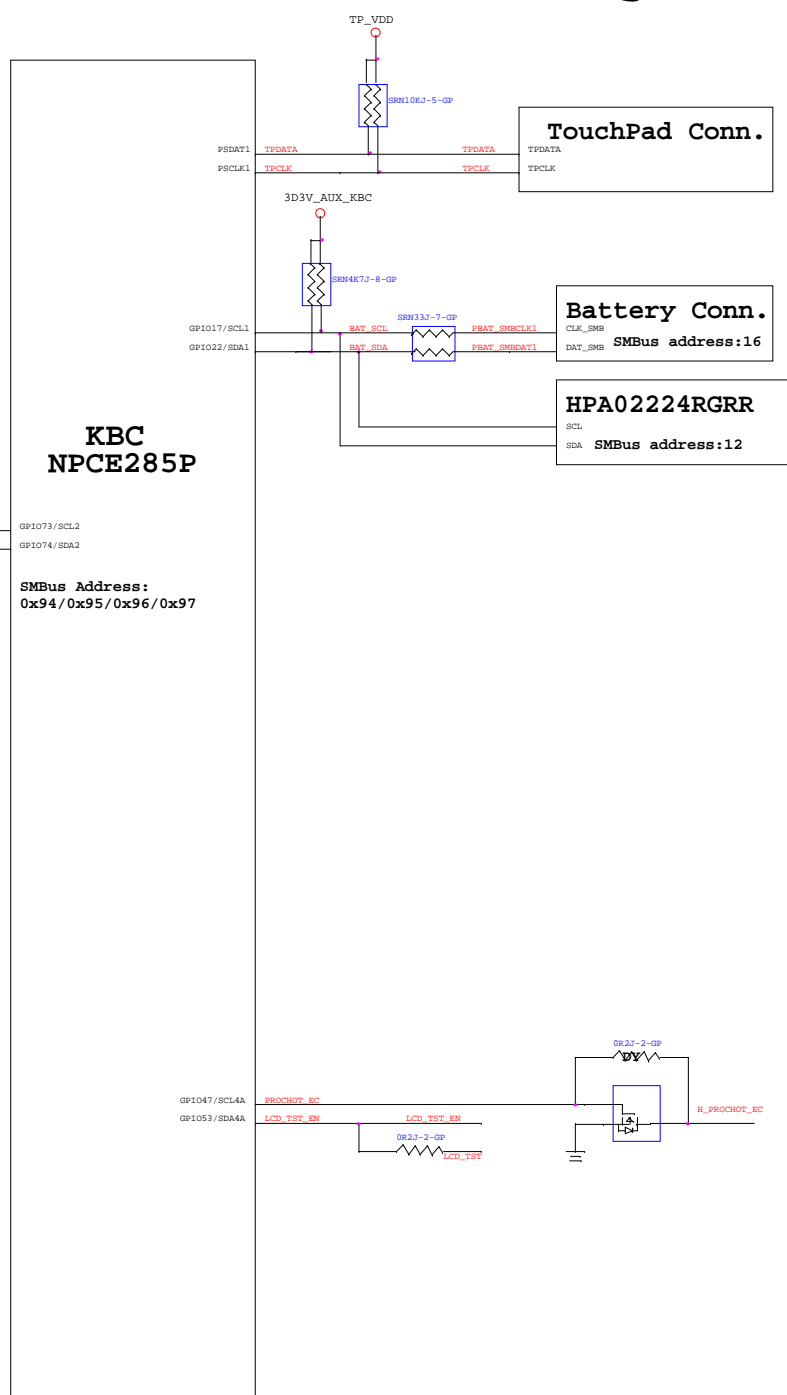


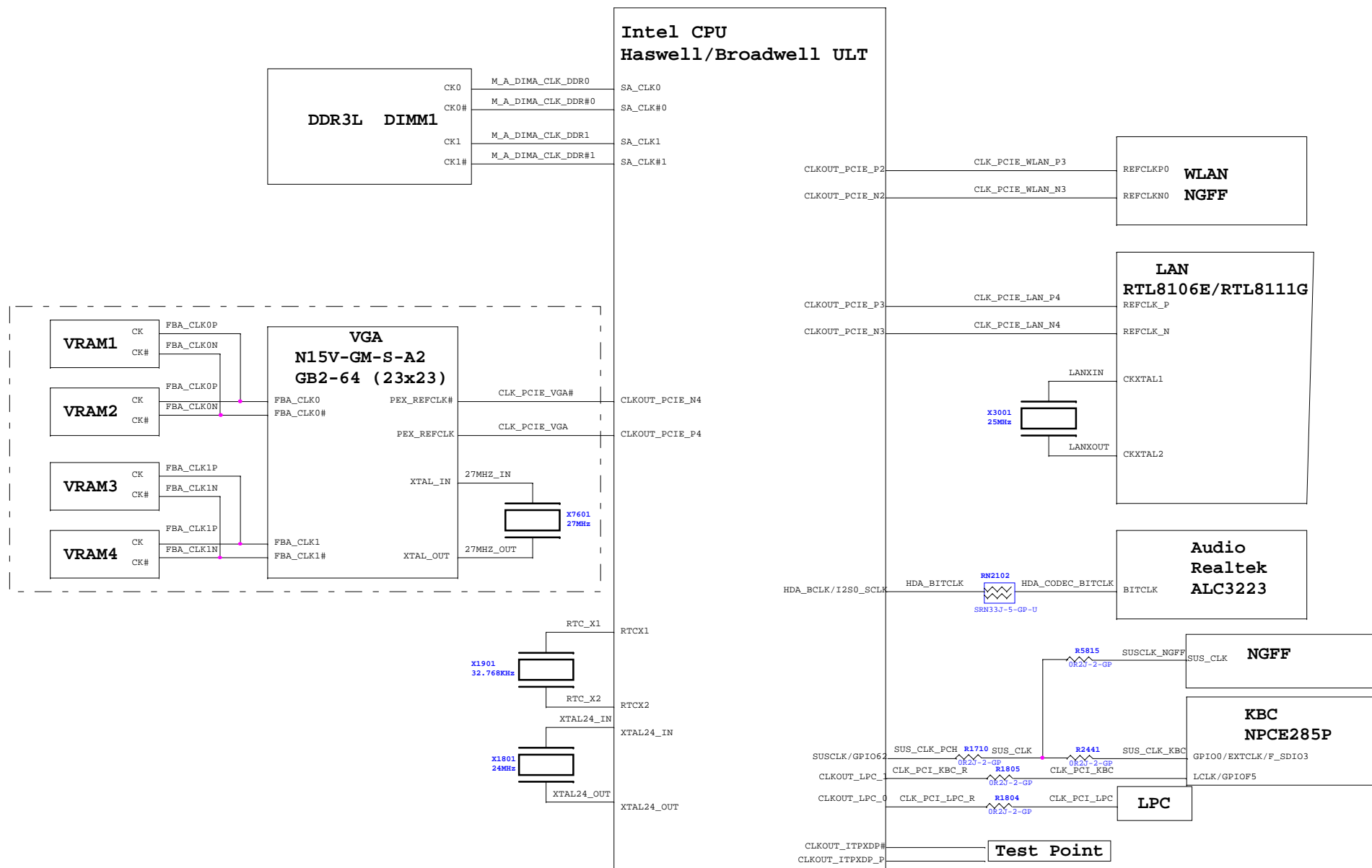
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FCH SMBus Block Diagram

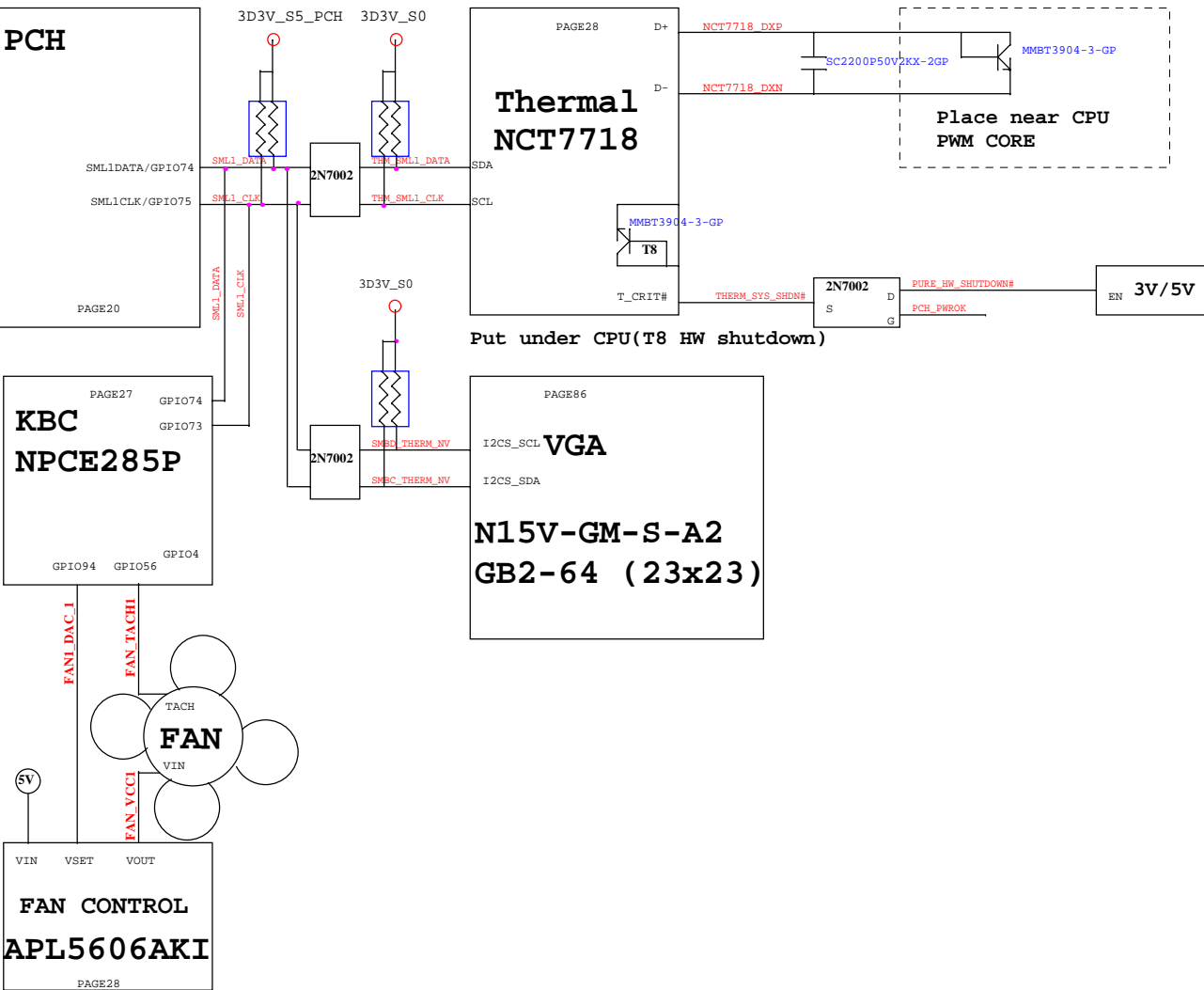


KBC SMBus Block Diagram

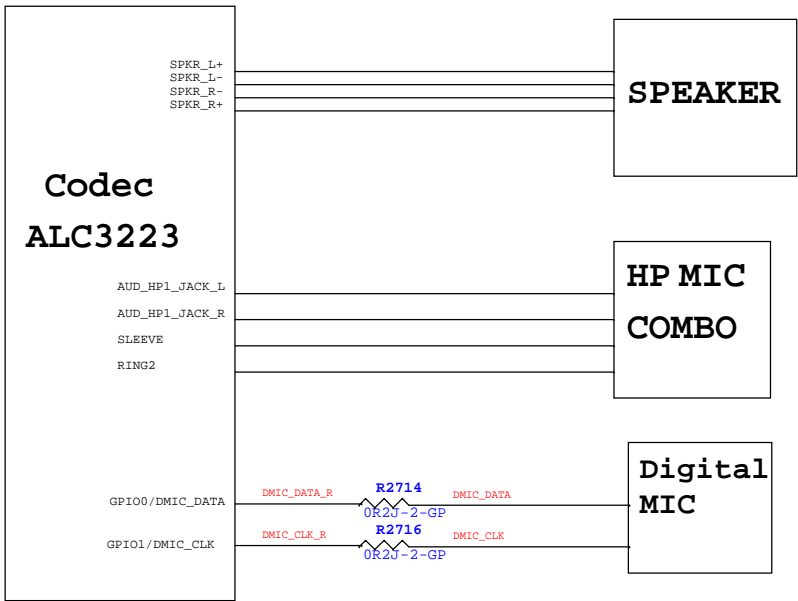





Thermal Block Diagram




Audio Block Diagram



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